

# USB4™ Logical Layer

## Compliance Test Specification for Router Assemblies

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Revision History:

Revision	Issue Date	Comments
1.0	June 2020	First Release
1.1	September 2020	With corrections and clarifications.
1.2	January 2021	With corrections and clarifications.
1.3	May 2021	With corrections and clarifications. References the USB4 Specification, Version 1.0 with Errata and ECN through October 15, 2020.
1.4	October 2021	With corrections and clarifications. References the USB4 Specification, Version 1.0 with Errata and ECN through May 19, 2021.
1.5	December 2021	With corrections and clarifications. References the USB4 Specification, Version 1.0 with Errata and ECN through May 19, 2021.
1.6	March 2022	With corrections and clarifications. References the USB4 Specification, Version 1.0 with Errata and ECN through May 19, 2021.
1.7	October 2022	With corrections and clarifications. References the USB4 Specification, Version 1.0 with Errata and ECN through May 19, 2021.
1.8	December 2022	With corrections and clarifications. References the USB4 Specification, Version 1.0 with Errata and ECN through May 19, 2021 and includes additional ECN through October 2022.
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1.10	September 2023	With corrections and clarifications. References the USB4 Specification, Version 1.0 with Errata and ECN through June 2023.
2.0	January 2024	First release with V2 tests.

2.4	February 2025	<p>Update Sideband Channel Background Check REG symbol values to allow for V2 additions</p> <p>TD 4.032 Part 1 update step 3 to start timer on SLOS or CL_WAKE1.X.</p> <p>TD 4.032 Part 2 update step 9 to start timer on SLOS or CL_WAKE1.X.</p> <p>TD 4.033 Part 1 update</p>
2.5	August 2025	<p>TD 4.005 remove Part 4 Step 14.k Bits[3:2](Reserved) are 0. This was V1-only.</p> <p>TD 4.005 add clarification to New Request processing in Part 4 18.d.</p> <p>TD 4.005 Part 4.21 and Part 4.22 correct step numbers inside test steps.</p> <p>TD 4.010 change requirement from 16 CL_NACK Ordered Sets to a margin of 10-40 Ordered Sets.</p> <p>TD 4.012 change requirement from 16 CL_NACK Ordered Sets to a margin of 10-40 Ordered Sets.</p> <p>TD 4.014 change requirement from 16 TS2 Ordered Sets to a margin of 10-40 Ordered Sets.</p> <p>TD 4.016 Part 3 remove Step e. tWakeResponse timing check</p> <p>TD 4.020 update to gather a 5ms trace, instead of 1 minute trace.</p> <p>TD 4.035 split bonding steps into UFP and DFP.</p>
2.6	October 2025	<p>TD 4.005 Part 3 Change SLOS1 verification to SLOS, to account for retimers on the link.</p> <p>TD 4.005 Part 4 Step 24 specify timing constraints. Previously TBD. This is not implemented yet.</p> <p>TD 4.105 Remove Part 1 and Part 2 step that verifies TSNOS from PUT if it is a DFP.</p> <p>TD 4.106 Remove Part 1 and Part 2 step that verifies TSNOS from PUT if it is a DFP.</p> <p>TD 4.010 Add margin to CL_NACK verification.</p> <p>TD 4.012 Add margin to CL_NACK verification.</p> <p>TD 4.014 Add margin for TS2 verification.</p> <p>TD 4.016 Remove tWakeResponse verification, as it is not possible to verify from the trace if there is a retimer on the link.</p> <p>Addition of tests TD 4.110, TD 4.115, TD 4.144</p>

		TBT3 Sideband Channel Background Check: Remove Bit 4 (Responder) from AT response check.
2.7	April 2026	<p>TD 4.010: Added new step in Part 3 to indicate that exerciser continues to send CL_NAK as long as it receives CL2_REQ.</p> <p>TD 4.011: Added new step in Part 3 to indicate that exerciser continues to send CL_NAK as long as it receives CL2_REQ.</p> <p>TD 4.012: Added new step in Part 3 to indicate that exerciser continues to send CL_NAK as long as it receives CL1_REQ or CL2_REQ.</p> <p>TD 4.013: Added new step in Part 3 to indicate that exerciser continues to send CL_NAK as long as it receives CL1_REQ or CL2_REQ.</p> <p>TD 4.016: Allow for CL_WAKE1.X in Part 1, CL0s exit.</p> <p>TD 4.035: Clarify Part 3 that the PUT must drive SBTX low.</p> <p>TD 4.052: Clarify that CLd is indicated by SB disconnect.</p> <p>TD 4.105: Part 1 Remove step regarding RS_FEC and UNBOND OSs, per base spec.</p> <p>TD 4.105: Part 2 Remove step regarding RS_FEC and UNBOND OSs, per base spec.</p> <p>TD 4.106: Part 1 Remove step regarding RS_FEC and UNBOND OSs, per base spec.</p> <p>TD 4.106: Part 2 Remove step regarding RS_FEC and UNBOND OSs, per base spec.</p> <p>TD 4.020: Add uni-directional Time Sync Handshake for Gen 4.</p> <p>TD 4.144: Clarify 1-symbol errors, not 1-byte errors</p>

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## Introduction

The tests in this specification verify that the Logical Layer of Router in a Router Assembly is compliant with the USB4™ Specification. If the Router Assembly contains one or more On-Board Re-timers, additional tests verify that the Logical Layer of the Re-timer(s) in the Router Assembly are compliant with the USB4 Re-timer Specification.

## Terminology

The following table describes the terms used in this document.

Compliance Device	A KG USB4 Device that is capable of performing Transport Layer Packet loopback. The KG USB4 Device is configured by USB4 CV (when USB4 CV is upstream of the UUT) or the Exerciser (when the Exerciser is upstream of the UUT). Unless specified otherwise, the Compliance Device is configured as an ordinary KG USB4 Device. See the USB4 Connection Manager Guide for more information on how a USB4 Device is configured.
DFP	Downstream Facing Port.
Exerciser	The compliance test tool (hardware and software) that implements USB4 Port functionality and the behavior required for compliance testing.
IOP	Interop Testing. See USB4™ Interop Test Specification.
KG USB4 Device	“Known Good” USB4 Device. A USB4 Device that is known to be compliant with the USB4 Specification.
KG USB4 Host	“Known Good” USB4 Host. A USB4 Host that is known to be compliant with the USB4 Specification.
KG TBT3 Device	A Certified Thunderbolt 3 Device.
KG TBT3 Host	A Certified Thunderbolt 3 Host.
PUT	Port Under Test. The USB4 Port on a UUT that is the test point for compliance testing.
UFP	Upstream Facing Port.
USB4 CV	USB4 Command Verifier software. The software that runs compliance tests and analyzes the results.
USB4 Product	Refers to a USB4 host, USB4 hub, and/or USB4 device. Includes silicon, reference platforms, and end product.
UUT	Unit Under Test. The Router Assembly that is being tested for compliance.
VIF	Vendor Information File. File provided by UUT vendor that provides information about the characteristics and capabilities of the UUT.

## Assertions

Compliance criteria are provided as a list of assertions that describe specific characteristics or behaviors that must be met. Each assertion provides a reference to the USB4™ specification or other documents from which the assertion was derived. In addition, each assertion provides a reference to the specific test description(s) where the assertion is tested.

Each test assertion is formatted as follows:

Assertion #	Test #	Assertion Description
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**Assertion#:** Unique identifier for each spec requirement. The identifier is in the form USB4\_SPEC\_SECTION\_NUMBER#X, where X is a unique integer for a requirement in that section.

**Assertion Description:** Specific requirement from the specification

**Test #:** A label for a specific test description in this specification that tests this requirement. Test # can have one of the following values:

NT	This item is not explicitly tested in a test description. Items can be labeled NT for several reasons – including items that are not testable, not important to test for interoperability, or are indirectly tested by other operations performed by the compliance test.
X.X	This item is covered by the test described in test description X.X in this specification.
IOP	This assertion is verified by the USB4 Interoperability Test Suite.
BC	This assertion is verified as part of a background check.

Test descriptions provide a high level overview of the tests that are performed to check the compliance criteria. The descriptions are provided with enough detail so that a reader can understand what the test does. The descriptions do not describe the actual step-by-step procedure to perform the test.

## Reserved Fields and Values

### Chapter 1

The following Table presents the USB4 Specification Chapter 1 asserts regarding reserved fields and values.

Assertion #	Test Name	Assertion Description
<b>1.7 Reserved Fields and Values</b>		
1.7#1	BC	A transmitter shall not use a value in this specification that is marked as “Rsvd”.
1.7#2	TD 4.052	The target of a Transaction shall ignore a Transaction that has any of its defined fields set to an Rsvd value and proceed as if the Transaction was never received.
1.7#3	TBD	A transmitter shall not use a value in this specification that is marked as “Rsvd”.
1.7#4	TBD	The target of an Ordered Set shall ignore an Ordered Set that has any of its defined fields set to an Rsvd value and proceed as if the Ordered Set was never received.
1.7#5	BC TD 4.005	A transmitter shall set a field that is marked “Rsvd” to zero.
1.7#6	TD 4.052	A receiver shall ignore any fields that are marked “Rsvd”.

## Ver. 1 Router Assertions

### Chapter 4

The following Table presents the USB4 Specification Chapter 4 asserts.

Assertion #	Test Name	Assertion Description
<b>4 Logical Layer</b>		
<b>4.1 Sideband Channel</b>		
<b>4.1.1 Transactions</b>		
<b>4.1.1.1 Symbols</b>		
4.1.1.1#1	IOP	A Sideband Channel shall encode all transmitted Symbols using the 10-bit Start/Stop encoding scheme as follows: A Start bit (logical 0b), Eight bits of payload, and A Stop bit (logical 1b).
<b>4.1.1.2 Transaction Types</b>		
4.1.1.2#1	IOP	The symbols within a transaction shall be sent in ascending order.
4.1.1.2#2	IOP	The bits within a symbol shall be sent in the order from bit 0 to bit 7.
<b>4.1.1.2.1 LT Transactions</b>		
4.1.1.2.1#1	BC	An LT Transaction shall consist of the three Symbols described in Table 4-1.
4.1.1.2.1#2	NT	Within a LSE Symbol: Bit 5 (LSELane) shall be 0b (for Lane 0) or 1b (for Lane 1).
4.1.1.2.1#3	BC	Within a LSE Symbol: Bit 5 (LSELane) shall be set to 0b when issuing an LT_LRoff Transaction.
4.1.1.2.1#4	BC	Within a LSE Symbol: Bits [7:6] (StartLT) shall be set to 10b.
4.1.1.2.1#5	0	The recipient of an LT Transaction shall verify that the CLSE Symbol payload is a bitwise complement of the LSE Symbol payload.
4.1.1.2.1#6	0	An LT Transaction that fails this check shall be dropped and no further action shall be taken on its behalf.
<b>4.1.1.2.2 AT Transactions</b>		
4.1.1.2.2#1	BC	An AT Transaction shall consist of the Symbols in Table 4-3.
4.1.1.2.2#2	BC	The number of Data Symbols (n) in an AT Transaction shall not exceed 66.

4.1.1.2.2#3	NT	Within a STX Symbol for an AT Transaction: Bit 0 ( <i>CmdNotResp</i> ) shall be set to 0b for an AT Response or 1b for an AT Command.
4.1.1.2.2#4	BC	Within a STX Symbol: Bit 1 ( <i>ReturnBounce</i> ) shall be set to 0b.
4.1.1.2.2#5	BC	Within a STX Symbol for an AT Transaction: Bit 2 ( <i>Recipient</i> ) shall be set to 1b.
4.1.1.2.2#6	BC	Within a STX Symbol for an AT Transaction: Bit 3 ( <i>Bounce</i> ) shall be set to 0b.
4.1.1.2.2#7	BC	Within a STX Symbol for an AT Transaction: Bit 4 ( <i>Responder</i> ) shall be set to 0b.
4.1.1.2.2#8	BC	Within a STX Symbol for an AT Transaction: Bits [7:6] ( <i>StartAT</i> ) shall be set to 00b.
4.1.1.2.2#9	BC	A Router that receives an AT Command with the Recipient bit set to 1b shall respond with an AT Response.
<b>4.1.1.2.3 RT Transactions</b>		
<b>4.1.1.2.3.1 Broadcast RT Transaction</b>		
4.1.1.2.3.1#1	BC	A Broadcast RT Transaction shall have the format shown in Table 4-5.
4.1.1.2.3.1#2	NT	Within a STX Symbol for a Broadcast RT Transaction: Bits [7:6] ( <i>StartRT</i> ) shall be set to 01b.
4.1.1.2.3.1#3	NT	Within a STX Symbol for a Broadcast RT Transaction: Bit 5 ( <i>Broadcast</i> ) shall be set to 1b.
4.1.1.2.3.1#4	BC TD 4.005	Within a STX Symbol for a Broadcast RT Transaction: Bits [4:1] ( <i>Index</i> ) shall be set to 0.
4.1.1.2.3.1#5	BC	Within a STX Symbol for a Broadcast RT Transaction: Bit 0 ( <i>CmdNotResp</i> ) shall be set to 1b.
4.1.1.2.3.1#6	BC	Within Byte 2 of a Broadcast RT Transaction: Bit 4 ( <i>TBT3-Compatible Speed</i> ) is set to 0b.
4.1.1.2.3.1#7	BC	Within Byte 2 of a Broadcast RT Transaction: Bit 0 ( <i>USB4</i> ) is set to 1b.
4.1.1.2.3.1#8	TD 4.005	Within Byte 3 of a Broadcast RT Transaction: Bit 1 ( <i>Lane1Enabled</i> ) shall equal the value of the Enabling Decision (Lane 1) bit in the Link Configuration register of the SB Register Space.
4.1.1.2.3.1#9	TD 4.005	Within Byte 3 of a Broadcast RT Transaction: Bit 0 ( <i>Lane0Enabled</i> ) shall equal the value of the Enabling Decision (Lane 0) bit in the Link Configuration register of the SB Register Space.

<b>4.1.1.2.3.2 Addressed RT Transaction</b>		
4.1.1.2.3.2#1	BC	An Addressed RT Transaction shall have the format shown in Table 4-9.
4.1.1.2.3.2#2	BC	The number of Data Symbols shall not exceed 66.
4.1.1.2.3.2#3	NT	Within a STX Symbol for an Addressed RT Transaction: Bits [7:6] ( <i>StartRT</i> ) shall be set to 01b.
4.1.1.2.3.2#4	NT	Within a STX Symbol for an Addressed RT Transaction: Bit 5 ( <i>Broadcast</i> ) shall be set to 0b.
4.1.1.2.3.2#5	NT	Within a STX Symbol for an Addressed RT Transaction: Bits [4:1] ( <i>Index</i> ) in an Addressed RT Command shall be set to 0 if the target of the Transaction is the first Router or Re-timer that receives the Transaction.
4.1.1.2.3.2#6	NT	Else, shall be set to the Re-timer Index of the Re-timer that is the target of the Command.
4.1.1.2.3.2#7	NT	Within a STX Symbol for an Addressed RT Transaction: Bit 0 ( <i>CmdNotResp</i> ) shall be set to 0b for an Addressed RT Response or 1b for an Addressed RT Command.
4.1.1.2.3.2#8	NT	A Router that receives an Addressed RT Command with the Index field set to 0 shall respond with an Addressed RT Response.
4.1.1.2.3.2#9	TD 4.001	A Router shall not respond to Addressed RT Commands with a non-zero Index field.
<b>4.1.1.2.4 AT and RT Transaction Rules</b>		
4.1.1.2.4#1	NT	A transmitter shall not abort an AT Transaction or an RT Transaction after the STX Symbol is sent.
4.1.1.2.4#2	TD 4.028	When a receiver receives two or more leading DLE symbols it shall discard the extra leading DLE symbols and process the received LT Transaction as if only one leading DLE symbol was received
4.1.1.2.4#3	TD 4.002	If any Data Symbol or a CRC Symbol in an AT Transaction or an RT Transaction contains the same payload as a DLE Symbol, the transmitter of the AT Transaction or RT Transaction shall insert a Symbol with payload of FEh in front of that Data Symbol.
4.1.1.2.4#4	TD 4.002	The recipient of an AT Transaction or an RT Transaction shall strip all duplicating FEh Symbols that immediately precede a Data Symbol or a CRC Symbol.
4.1.1.2.4#5	BC	Each AT Transaction or RT Transaction shall include a 16-bit CRC.
4.1.1.2.4#6	BC	Only the STX and Data Symbols shall be used in CRC calculation.

4.1.1.2.4#7	BC	The CRC shall be calculated in increasing Symbol order, starting with the STX Symbol.
4.1.1.2.4#8	BC	Within each Symbol, CRC shall be calculated from bit[7] to bit[0].
4.1.1.2.4#9	BC	The CRC shall be calculated using the following rules: Width: 16; Poly: 8005h; Init: FFFFh; RefIn: True; RefOut: True; XorOut: 0000h.
<b>4.1.1.2.5 AT and RT Command Rules</b>		
4.1.1.2.5#1	IOP	A Router shall process AT Commands and AT Responses arriving from the Link Partner or Re-timer in the order received.
4.1.1.2.5#2	IOP	A Router shall process Addressed RT Commands and Addressed RT Responses arriving from a Re-timer in the order received.
4.1.1.2.5#3	TD 4.004	A Router shall not send an AT Command or Addressed RT Command while it is waiting for a response for either a previously sent AT Command or a previously sent Addressed RT Command.
<b>4.1.1.2.5.1 AT Commands</b>		
4.1.1.2.5.1#1	BC	The recipient of an AT Command shall send an AT Response within tCmdResponse of receiving the AT Command.
4.1.1.2.5.1#2	NT	If a Router sends an AT Command, then receives at least two AT Commands from the target of the outstanding AT Command within tATTimeout, it shall stop waiting for an AT Response and shall immediately reissue the outstanding AT Command.
4.1.1.2.5.1#3	TD 4.004	Otherwise, a Router shall wait tATTimeout for an AT Response.
<b>4.1.1.2.5.2 Addressed RT Commands</b>		
4.1.1.2.5.2#1	BC	The recipient of an Addressed RT Command shall send an Addressed RT Response within tCmdResponse of receiving the Addressed RT Command.
4.1.1.2.5.2#2	TD 4.004	A Router shall wait tRTTimeout for an Addressed RT Response.
<b>4.1.1.2.6 Receiver Decoding of LT, AT, and RT Transactions</b>		
4.1.1.2.6#1	TD 4.029	A Router shall ignore and discard an AT Transaction or an Addressed RT Transaction if any of the following are true: The CRC in the Transaction is invalid.
4.1.1.2.6#2	TD 4.029	A Router shall ignore and discard an AT Transaction or an Addressed RT Transaction if any of the following are true: The Transaction has no data and no CRC field.
4.1.1.2.6#3	TD 4.029	Any sequence of Symbols not handled as an LT Transaction, an AT Transaction, or an RT Transaction shall be discarded.



4.1.1.2.6#4	TD 4.029	An AT Response or an RT Response shall not be sent in response to such a sequence.
<b>4.1.1.3 SB Register Space</b>		
4.1.1.3#1	NT	A Router shall maintain one SB Register Space per USB4 Port.
<b>4.1.1.3.1 Router Access</b>		
4.1.1.3.1#1	BC	An AT Command or RT Command shall consist of the Symbols described in Table 4-12.
4.1.1.3.1#2	BC	In an AT or RT Command, LEN shall not be greater than 64.
4.1.1.3.1#3	IOP	For a Write Command, COMMAND_DATA register Contents shall appear least significant byte first.
4.1.1.3.1#4	BC	An AT Response or RT Response shall consist of the Symbols described in Table 4-13.
4.1.1.3.1#5	IOP	For a Read Response, RESPONSE_DATA register contents shall appear low-ordered byte first.
4.1.1.3.1#6	TD 4.030	When a Router receives an AT Command or an RT Command, it shall process the AT or RT Command according to Table 4-14 and in the order listed: Operation with a single Data Symbol, send a Response with no RESPONSE_DATA and LEN set to 0.
4.1.1.3.1#7	TD 4.030	When a Router receives an AT Command or an RT Command, it shall process the AT or RT Command according to Table 4-14 and in the order listed: Read operation to an unsupported vendor defined register or to an undefined register, send a Response with no RESPONSE_DATA and LEN set to 0.
4.1.1.3.1#8	TD 4.030	When a Router receives an AT Command or an RT Command, it shall process the AT or RT Command according to Table 4-14 and in the order listed: Read operation with more than two Data Symbols, send a Response with no RESPONSE_DATA and LEN set to 0.
4.1.1.3.1#9	TD 4.030	When a Router receives an AT Command or an RT Command, it shall process the AT or RT Command according to Table 4-14 and in the order listed: Read operation of more bytes than the target register length, send a Response with the entire register contents in the RESPONSE_DATA and LEN set to the number of bytes in the RESPONSE_DATA field.
4.1.1.3.1#10	TD 4.030	When a Router receives an AT Command or an RT Command, it shall process the AT or RT Command according to Table 4-14 and in the order listed: Read operation of fewer bytes than the target register length, send a Response with the number of bytes requested in the RESPONSE_DATA and LEN set to the size in bytes of the target register being accessed.

4.1.1.3.1#11	IOP	When a Router receives an AT Command or an RT Command, it shall process the AT or RT Command according to Table 4-14 and in the order listed: All other read operations, perform the Read Command and send a Read Response with the contents of the register being accessed in the RESPONSE_DATA field.
4.1.1.3.1#12	TD 4.003	When a Router receives an AT Command or an RT Command, it shall process the AT or RT Command according to Table 4-14 and in the order listed: Write operation to an unsupported vendor defined register or to an undefined register, do not perform the Write Command, send a Response with the LEN field = 0 and the Result Code = 01h (ERROR) in the RESPONSE_DATA field.
4.1.1.3.1#13	TD 4.003	When a Router receives an AT Command or an RT Command, it shall process the AT or RT Command according to Table 4-14 and in the order listed: Write operation with LEN field that does not match the Transaction size, do not perform the Write Command, send a Response with the LEN field = 0 and the Result Code = 01h (ERROR) in the RESPONSE_DATA field.
4.1.1.3.1#14	TD 4.003	When a Router receives an AT Command or an RT Command, it shall process the AT or RT Command according to Table 4-14 and in the order listed: Write operation to a Read-only (RO) register, do not perform the Write Command, a send a Response with the LEN field = 0 and the Result Code = 01h (ERROR) in the RESPONSE_DATA field.
4.1.1.3.1#15	TD 4.003	When a Router receives an AT Command or an RT Command, it shall process the AT or RT Command according to Table 4-14 and in the order listed: Write operation of more bytes than the target register length, do not perform the Write Command, send a Response with the LEN field = 0 and the Result Code = 01h (ERROR) in the RESPONSE_DATA field.
4.1.1.3.1#16	TD 4.003	When a Router receives an AT Command or an RT Command, it shall process the AT or RT Command according to Table 4-14 and in the order listed: Write operation of less bytes than the target register length, perform the write operation only on the requested bytes, send a Response with the LEN field equal to the size in bytes of the register being accessed and the Result Code = 00h (SUCCESS) in the RESPONSE_DATA field.
4.1.1.3.1#17	IOP	When a Router receives an AT Command or an RT Command, it shall process the AT or RT Command according to Table 4-14 and in the order listed: All other write operations, perform the Write Command and send a Response with the LEN field equal to the size in bytes of the register being accessed and the Result Code = 00h (SUCCESS) in the RESPONSE_DATA field.
<b>4.1.1.3.2 Connection Manager Access</b>		
4.1.1.3.2#1	NT	When the <i>Pending</i> bit in a USB4 Port Capability is set to 1b, a Router shall: If the <i>Target</i> field in the USB4 Port Capability is set to 000b, the Router shall issue an access to the SB Register Space of the Port.
4.1.1.3.2#2	NT	The Router shall access the register identified in the <i>Address</i> field in the USB4 Port Capability.

4.1.1.3.2#3	NT	The Router shall access the number of bytes indicated in the <i>Length</i> field.
4.1.1.3.2#4	NT	If the <i>WnR</i> field is set to 0b, the Router shall read from the SB Register Space.
4.1.1.3.2#5	NT	If the <i>WnR</i> field is set to 1b, the Router shall write to the SB Register Space.
4.1.1.3.2#6	NT	The Router shall write the contents from the <i>Data</i> DWs in the USB4 Port Capability.
4.1.1.3.2#7	NT	Register contents shall be written least significant byte first.
4.1.1.3.2#8	NT	When the <i>Pending</i> bit in a USB4 Port Capability is set to 1b, a Router shall: If the <i>Target</i> field in the USB4 Port Capability is set to 001b, the Router shall send an AT Command on the Sideband Channel of the Port to access the SB Register Space of the Link Partner.
4.1.1.3.2#9	NT	The AT Command shall have the following contents: The <i>REG</i> field shall be set to the contents of the <i>Address</i> field in the USB4 Port Capability.
4.1.1.3.2#10	NT	The AT Command shall have the following contents: The <i>LEN</i> field shall be set to the contents of the <i>Length</i> field in the USB4 Port Capability.
4.1.1.3.2#11	NT	The AT Command shall have the following contents: The <i>WnR</i> field shall be set to the contents of the <i>WnR</i> field in the USB4 Port Capability.
4.1.1.3.2#12	NT	The AT Command shall have the following contents: If the <i>WnR</i> field is set to 1b, the COMMAND_DATA Symbols shall contain the contents from the <i>Data</i> DWs in the USB4 Port Capability. Register contents shall appear least significant byte first.
4.1.1.3.2#13	NT	When the <i>Pending</i> bit in a USB4 Port Capability is set to 1b, a Router shall: If the <i>Target</i> field in the USB4 Port Capability is set to 010b, the Router shall send an Addressed RT Command on the Sideband Channel of the Port to access the SB Register Space of a Re-timer on the Link.
4.1.1.3.2#14	NT	The Addressed RT Command shall have the following contents: The <i>Index</i> field in an Addressed RT Command shall be set to the contents of the Re-timer Index in the USB4 Port Capability.
4.1.1.3.2#15	NT	The Addressed RT Command shall have the following contents: The <i>REG</i> field in an Addressed RT Command shall be set to the contents of the <i>Address</i> field in the USB4 Port Capability.
4.1.1.3.2#16	NT	The Addressed RT Command shall have the following contents: The <i>LEN</i> field in an Addressed RT Command shall be set to the contents of the <i>Length</i> field in the USB4 Port Capability.
4.1.1.3.2#17	NT	The Addressed RT Command shall have the following contents: The <i>WnR</i> field in an Addressed RT Command shall be set to the contents of the <i>WnR</i> field in the USB4 Port Capability.

4.1.1.3.2#18	NT	The Addressed RT Command shall have the following contents: If the <i>WnR</i> field in an Addressed RT Command is set to 1b, the <i>COMMAND_DATA</i> Symbols shall contain the contents from the <i>Data</i> DWs in the USB4 Port Capability. Register contents shall appear least significant byte first.
4.1.1.3.2#19	NT	A Router shall process an AT Command as described in Table 4-14.
4.1.1.3.2#20	NT	When a response to a local access is ready or when a Response Transaction is received, the Router shall update the USB4 Port Capability as follows: The <i>LEN</i> field in the AT Response, the RT Response, or the local access is copied to the <i>Length</i> field in the USB4 Port Capability.
4.1.1.3.2#21	TD 4.004	When a response to a local access is ready or when a Response Transaction is received, the Router shall update the USB4 Port Capability as follows: The <i>No Response</i> bit is updated.
4.1.1.3.2#22	NT	When a response to a local access is ready or when a Response Transaction is received, the Router shall update the USB4 Port Capability as follows: The <i>Result Code</i> bit in the USB4 Port Capability is updated.
4.1.1.3.2#23	NT	When a response to a local access is ready or when a Response Transaction is received, the Router shall update the USB4 Port Capability as follows: For a read, the <i>Data</i> DWs in the USB4 Port Capability are updated.
4.1.1.3.2#24	TD 4.004	The Router shall then set the <i>Pending</i> bit in the USB4 Port Capability to 0b.
<b>4.1.1.3.3 SB Register Definitions</b>		
4.1.1.3.3#1	TD 4.003	A Write operation to a field with the RO access type shall have no effect.
4.1.1.3.3#2	NT	A Read operation to a field with the RO access type shall return a meaningful value.
4.1.1.3.3#3	NT	A field with the RW access type shall be capable of both Read operation and Write operation.
4.1.1.3.3#4	NT	The value read from a field with RW access type shall reflect the last value written to it unless the field was reset in the interim.
4.1.1.3.3#5	NT	A Write operation to a Rsvd field shall have no effect.
4.1.1.3.3#6	TD 4.005	The SB Register Space registers shall have the structure and fields described in Table 4-17.
4.1.1.3.3#7	NT	Registers not listed in Table 4-17 are undefined and shall not be used.
4.1.1.3.3#8	TD 4.005	The Vendor ID Low field shall contain the same value as the lower byte of the Vendor ID field in Router Configuration Space.
4.1.1.3.3#9	TD 4.005	The Vendor ID High field shall contain the same value as the higher byte of the Vendor ID field in Router Configuration Space.

4.1.1.3.3#10	TD 4.005	The Product ID Low field shall contain the same value as the lower byte of the Device ID field in Router Configuration Space.
4.1.1.3.3#11	TD 4.005	The Product ID High field shall contain the same value as the higher byte of the Device ID field in Router Configuration Space.
4.1.1.3.3#12	CH8	A Router shall write the Completion Metadata (if any) to the Metadata field after executing a Port Operation.
4.1.1.3.3#13	TD 4.005	The Enabling Decision (Lane 0) field shall indicate whether or not Lane 0 is enabled during Lane Initialization: 0b = Adapter is in CLd state and 1b = Lane is Enabled.
4.1.1.3.3#14	TD 4.005	The Enabling Decision (Lane 1) field shall indicate whether or not Lane 1 is enabled during Lane Initialization: 0b = Adapter is in CLd state and 1b = Lane is Enabled.
4.1.1.3.3#15	TD 4.005	A Router shall set the Enabling Request (Lane 0) bit to 0b when the Lane Disable bit in the USB4 Adapter Configuration Capability for Lane 0 is 1b. Otherwise this bit shall be set to 0b.
4.1.1.3.3#16	NT	A Lane 1 Adapter shall not request enabling unless the Lane 0 Adapter requests enabling.
4.1.1.3.3#17	NT	Deprecated.
4.1.1.3.3#18	NT	A Router shall set the Enabling Request (Lane 1) bit to 0b when the Lane Disable bit in the USB4 Adapter Configuration Capability for Lane 1 is 1b. Otherwise this bit shall be set to 1b. Otherwise this bit shall be set to 1b.
4.1.1.3.3#19	NT	A USB4 Port shall only set the <i>Gen 3 Support</i> bit to 1b if all of the following are true: The Port supports Gen 3 speeds; All On-Board Re-timers connected between the Port and the cable support Gen 3 speeds; The Port implements both a Lane 0 Adapter and a Lane 1 Adapter; The Target Link Speed field in the Lane Adapter Configuration Capability is 1100b.
4.1.1.3.3#20	NT	Otherwise the <i>Gen 3 Support</i> bit shall be 0b.
4.1.1.3.3#21	NT	A USB4 Port shall set the RS-FEC Request (Gen 2) bit to the same value as the Request RS-FEC Gen 2 bit in the USB4 Port Capability.
4.1.1.3.3#22	NT	A USB4 Port shall set the RS-FEC Request (Gen 3) bit to the same value as the Request RS-FEC Gen 3 bit in the USB4 Port Capability.
4.1.1.3.3#23	TD 4.005	The USB4 Sideband Channel field shall be set to 1b.
4.1.1.3.3#24	TD 4.005	A USB4 Port shall only set the TBT3-Compatible Speeds Supported bit to 1b if all On-Board Re-timers connected between the Router and the cable support TBT3-compatible speeds.
4.1.1.3.3#25	TD 4.005	Bit 2 through 7 of byte 2 in the Link Configuration register are 0 (reserved).

4.1.1.3.3#26	TD 4.005	The <i>Clock Switch Done (Lane 0)</i> bit shall be set to the value of the Rx Locked (Lane 0) bit.
4.1.1.3.3#27	TD 4.005	The <i>Clock Switch Done (Lane 1)</i> bit shall be set to the value of the Rx Locked (Lane 1) bit.
4.1.1.3.3#28	CH8	A Router shall write the Completion Data (if any) to the <i>Data</i> field after executing a Port Operation.
<b>4.1.2 Lane Initialization</b>		
4.1.2#1	IOP	The Sideband Channel shall initialize each Lane independently.
4.1.2#2	IOP	Initialization shall occur for all enabled USB4 Ports on a Router.
<b>4.1.2.1 Phase 1 – Determination of Initial Conditions</b>		
4.1.2.1#1	NT	A USB4 Port shall not continue on to Phase 2 until it has obtained the connection information described in this section.
4.1.2.1#2	NT	A USB4 Port shall not proceed to Phase 2 if the Link is not USB4.
4.1.2.1#3	NT	A USB4 Port shall drive SBTX to logic low by default.
<b>4.1.2.1.1 Lane Reversal</b>		
4.1.2.1.1#1	IOP	When a Router detects a reverse insertion on a USB Type-C connector, it shall perform Lane Reversal in the USB4 Port that faces the reversed connector.
4.1.2.1.1#2	IOP	Lane Reversal shall be performed during phase 1.
4.1.2.1.1#3	IOP	The Router shall swap the designation of Lane 0 and Lane 1 and shall associate the Lane 0 Adapter with the updated Lane 0 and the Lane 1 Adapter with the updated Lane 1.
4.1.2.1.1#4	IOP	If there are no On-Board Re-timers between Router and the USB Type-C connector, the Router shall swap its SBTX and SBRX lines facing the connector.
<b>4.1.2.1.2 Polarity Inversion</b>		
<b>4.1.2.2 Phase 2 – Router Detection</b>		
4.1.2.2#1	TD 4.005	After completion of phase 1, a Host Router shall initiate Router detection by driving SBTX to logic high on all of its Downstream Facing Ports.
4.1.2.2#2	TD 4.005	When a Device Router detects a logic high on SBRX of its Upstream Facing Port for tConnectRx time, it shall drive SBTX to logic high on all of its USB4 Ports.

4.1.2.2#3	NT	After a USB4 Port drives its SBTX to logic high and detects a logic high on its SBRX for tConnectRx time, it shall set its <i>Link Initialization in Progress</i> bit to 1b, then transition to Phase 3 of Lane Initialization.
<b>4.1.2.3 Phase 3 – Determination of USB4 Port Characteristics</b>		
4.1.2.3#1	TD 4.005	During phase 3, Router A shall read the Link Configuration Register (register 12) of Router B using AT Transactions.
4.1.2.3#2	TD 4.005	Router A shall issue at least one more register read to Router B in order to avoid a tATTimeout delay at the Link Partner.
4.1.2.3#3	NT	(Enabling) If Enabling Request = 1b in the SB Register Space of the Ports of both Router A and Router B, Router A shall: proceed to initialize the Lane.
4.1.2.3#4	TD 4.005	(Enabling) If Enabling Request = 1b in the SB Register Space of the Ports of both Router A and Router B, Router A shall: set the local Enabling Decision bit for the Lane to 1b.
4.1.2.3#5	NT	(Enabling) Else, Router A shall not initialize the Lane. The Lane shall remain in CLd state.
4.1.2.3#6	TD 4.005	(Enabling) Else, Router A shall set the local Enabling Decision bit for the Lane to 0b.
4.1.2.3#7	TD 4.005	(Dual-Lane) Router A shall set the Bonding Enabled bit in the USB4 Port Capability to 1b if all of the following are true: The USB4 Ports of Router A and Router B both have the Enabling Request bit set to 1b for both Lanes of the USB4 Port; The USB4 Ports of Router A and Router B both support Lane bonding (i.e. the Bonding Support bit is 1b in the SB Register Space of the Ports on both sides of the Lane).
4.1.2.3#8	TD 4.005	(Dual-Lane) Otherwise, Router A shall set Bonding Enabled bit to 0b.
4.1.2.3#9	IOP	(Speed) Router A shall operate at Gen 3 Lane speed if all of the following are true: The Ports on both sides of the Lane support Gen 3 ( <i>Gen 3 Support</i> is set to 1b); The cable over which Router A and Router B are communicating supports Gen 3.
4.1.2.3#10	IOP	(Speed) Otherwise, Router A shall operate at Gen 2 Lane Speed.
4.1.2.3#11	TD 4.005	(Speed) Router A shall set the Current Link Speed field in the USB4 Adapter Configuration Capability to reflect whether it is operating at Gen 2 or Gen 3 Lane speed.
4.1.2.3#12	IOP	(RS-FEC) At Gen 2 speed, Router A shall enable RS-FEC if both sides of the Link request it (i.e. the <i>RS-FEC Request (Gen 2)</i> bit is set to 1b in the SB Register Space of both the local USB4 Port and its Link Partner).
4.1.2.3#13	IOP	(RS-FEC) Otherwise, RS-FEC shall not be enabled.

4.1.2.3#14	TD 4.005	(RS-FEC) For Gen 2 speed, Router A shall set the RS-FEC Enabled (Gen 2) bit in the USB4 Port Capability to reflect whether it is operating with RS-FEC.
4.1.2.3#15	IOP	(RS-FEC) For Gen 3 speed, shall enable RS-FEC if both sides of the Link request it (i.e. the <i>RS-FEC Request (Gen 3)</i> bit is set to 1b in the SB Register Space of both the local USB4 Port and its Link Partner).
4.1.2.3#16	IOP	(RS-FEC) Otherwise, RS-FEC shall not be enabled.
4.1.2.3#17	TD 4.005	(RS-FEC) For Gen 3 speed, Router A shall set the RS-FEC Enabled (Gen 3) bit in the USB4 Port Capability to reflect whether it is operating with RS-FEC.
<b>4.1.2.4 Phase 4 – Lane Parameters Synchronization and Transmit Start</b>		
4.1.2.4#1	TD 4.005 TD 4.031	(Step 1) Router A shall send a Broadcast RT Transaction every tLaneParams with the parameter values in Table 4-18.
4.1.2.4#2	TD 4.005 TD 4.031	(Step 1) Router A shall continue sending Broadcast RT Transactions until all of the following conditions are true, then continue to step 2): At least tLTPhase4 time has passed from completion of Phase 2; Router A has sent Broadcast RT Transactions at least twice; Router A has received a Broadcast RT Transaction from Router B.
4.1.2.4#3	TD 4.005	(Step 2) Router A shall activate the transmitter on each enabled Lane at the selected speed and shall send SLOS1.
4.1.2.4#4	TD 4.005	(Step 3) After its transmitter is transmitting a valid signal, Router A shall then send an LT_Resume Transaction for each enabled Lane in the USB4 Port and shall set to 1b the Tx Active bit in the Tx Status byte of the TxFFE Register in the SB Register Space to indicate that it has started transmission on the target Lane.
4.1.2.4#5	TD 4.005	(Step 3) The LSELane field in the LT_Resume Transaction shall equal the Lane number associated with the transmitter.
<b>4.1.2.5 Phase 5 – Link Equalization</b>		
4.1.2.5#1	TD 4.005	Router A's transmitter shall perform the transmitter flow in the symmetric equalization flow defined in Section 4.1.2.5.1.1.
4.1.2.5#2	TD 4.005	A Router shall use Addressed RT Transactions with the <i>Index</i> field set to 0 to access the SB Register Space of the adjacent component, which can be either an On-Board Re-timer, a Cable Re-timer, or Router B.
4.1.2.5#3	TD 4.005	Router B's receiver shall perform the receiver flow in the symmetric equalization flow defined in Section 4.1.2.5.1.2.
4.1.2.5#4	TD 4.005	The Router shall use Addressed RT Transactions with the <i>Index</i> field set to 0b to access the SB Register Space of the adjacent component, which can be either an On-Board Re-timer, a Cable Re-timer, or Router A.



4.1.2.5#5	TD 4.005	A Router shall set the Clock Switch Done bit to 1b in the SB Register space of the Ports of a USB4 Port after all of the USB4 Port's receivers complete the equalization flow.
<b>4.1.2.5.1 Phase 5 – Symmetric TxFFE Negotiation</b>		
<b>4.1.2.5.1.1 Phase 5 – Transmitter Flow</b>		
4.1.2.5.1.1#1	NT	(Step 1) The transmitter shall start with the following default values in the Tx Status byte of the TxFFE register: Tx Active bit = 1b; Request Done bit = 0b.
4.1.2.5.1.1#2	TD 4.005	(Step 2) The transmitter shall read the <i>Rx Status &amp; TxFFE Request</i> byte of the receiver.
4.1.2.5.1.1#3	TD 4.005	(Step 3) On reception of a Response from the receiver, The transmitter shall do the following: If Rx Locked = 1, then negotiation is complete and no further TxFFE negotiation steps are taken; Else, if New Request = 0, the receiver has not provided a new request yet. The transmitter shall retry step 2 within tPollTXFFE of receiving the Response; Else, this is a new request to update TxFFE parameters. Continue on to step 4.
4.1.2.5.1.1#4	TD 4.005	(Step 4) The transmitter shall update its transmitter parameters based on the new parameters in the received Response.
4.1.2.5.1.1#5	TD 4.005	(Step 4) The transmitter shall update its Tx Status byte with the following values: TxFFE Setting = the index (from 16 possible values) loaded above to the TxFFE configuration configured at the transmitter; Request Done = 1b.
4.1.2.5.1.1#6	TD 4.005	(Step 5) The transmitter shall read the <i>Rx Status &amp; TxFFE Request</i> byte of the receiver.
4.1.2.5.1.1#7	TD 4.005	(Step 6) On reception of a Response from the receiver, the transmitter shall do the following: If New Request = 1, the receiver is still trying to lock on a previous request. The transmitter shall retry step 5 within tPollTXFFE of receiving the Response; Else, the transmitter shall set the Request Done bit in the Tx Status byte to 0b, and return to step 2.
<b>4.1.2.5.1.2 Phase 5 – Receiver Flow</b>		
4.1.2.5.1.2#1	NT	(Step 1) The receiver shall start with the following default values in the <i>Rx Status &amp; TxFFE Request</i> byte of the TxFFE register: Rx Locked bit = 0b; New Request bit = 1b; Rx Active bit = 0b.
4.1.2.5.1.2#2	TD 4.005	(Step 2) The receiver shall read the transmitter's Tx Status byte.
4.1.2.5.1.2#3	TD 4.005	(Step 3) On reception of a Response from the transmitter, the receiver shall do the following: If Tx Active = 1b, then enable the receiver, set Rx Active to 1b, and continue on to Step 4; Else, repeat step 2 within tPollTXFFE of receiving the Response.

4.1.2.5.1.2#4	TD 4.005	(Step 4) The receiver shall evaluate its receiver behavior and shall set the Rx Locked bit to 1b if equalization is complete.
4.1.2.5.1.2#5	TD 4.005	(Step 5) The receiver shall do the following: If Rx Locked = 1, then TXFFE negotiation is complete and no further negotiation steps are taken.
4.1.2.5.1.2#6	TD 4.005	(Step 5) The receiver shall do the following: If Rx Locked = 0, the receiver shall: Select a new set of TxFFE parameters and set the TxFFE Request field to the index of the selected set of TXFFE parameters; Set the New Request bit to 1b; Continue with the steps below.
4.1.2.5.1.2#7	TD 4.005	(Step 6) The receiver shall read the transmitter's Tx Status byte.
4.1.2.5.1.2#8	TD 4.005	(Step 7) On reception of a Response from the transmitter, the receiver shall do the following: If (Tx Active = 1b) AND (Request Done = 1b) AND (TxFFE Setting = value of TxFFE request in the local <i>Rx Status &amp; TxFFE Request</i> byte), then continue on to Step 8.
4.1.2.5.1.2#9	TD 4.005	(Step 7) On reception of a Response from the transmitter, the receiver shall do the following: If (Tx Active = 0b) OR (Request Done = 0b) OR (TxFFE Setting != value of TxFFE request in the local <i>Rx Status &amp; TxFFE Request</i> byte), repeat step 5 within tPollTXFFE of receiving the Response.
4.1.2.5.1.2#10	NT	(Step 8) The receiver shall evaluate its receiver behavior and set the Rx Locked bit to 1b if equalization is complete.
4.1.2.5.1.2#11	TD 4.005	(Step 9) The receiver shall set the New Request bit to 0b.
4.1.2.5.1.2#12	TD 4.005	(Step 10) The receiver shall read the transmitter's Tx Status byte by sending a read Command to the transmitter that targets its TxFFE register.
4.1.2.5.1.2#13	TD 4.005	(Step 11) On reception of a Response from the transmitter, the receiver shall do the following: If (Tx Active = 1b) and (Request Done = 0b), then go to Step 4.
4.1.2.5.1.2#14	TD 4.005	(Step 11) On reception of a Response from the transmitter, the receiver shall do the following: If (Tx Active = 0b) or (Request Done = 1b), repeat Step 9 within tPollTXFFE of receiving the Response.
<b>4.2 Logical Layer State Machine</b>		
<b>4.2.1 Lane Adapter State Machine</b>		
<b>4.2.1.1 Disabled</b>		
<b>4.2.1.1.1 Entry to State</b>		
4.2.1.1.1#1	TD 4.006	An Adapter shall enter this state from Training state or CL0 state when the <i>Lane Disable</i> bit in the Lane Adapter Configuration Capability is set to 1b.
4.2.1.1.1#2	TD 4.006	A Lane Adapter shall set the <i>Plugged</i> bit to 0b upon transitioning to Disabled state.

<b>4.2.1.1.2 Behavior in State</b>		
<b>4.2.1.1.1.3 Exit from State</b>		
4.2.1.1.3#1	NT	An Adapter shall exit this state when the <i>Lane Disable</i> bit in the Lane Adapter Configuration Capability is set to 0b
4.2.1.1.3#2	NT	A disabled Adapter shall stay in the Disabled state for a minimum of tDisabled.
4.2.1.1.3#3	NT	If the <i>Lane Disable</i> bit is set to 0b less than tDisabled after sending the LT_Fall Transaction, the Adapter shall not transition to the CLd state until tDisabled has elapsed.
<b>4.2.1.2 CLd</b>		
<b>4.2.1.2.1 Entry to State</b>		
4.2.1.2.1#1	NT	An Adapter shall enter this state on any of the following events: Router power on.
4.2.1.2.1#2	NT	An Adapter shall enter this state on any of the following events: The USB4 Port is disconnected and <i>Lane Disable</i> bit in the Lane Adapter Configuration Capability is set to 0b.
4.2.1.2.1#3	NT	An Adapter shall enter this state on any of the following events: Router enters Sleep state.
4.2.1.2.1#4	NT	In addition to the events listed above, a Lane Adapter that is not the Upstream Adapter shall enter this state on any of the following events: Adapter exits from the Disabled state.
4.2.1.2.1#5	NT	In addition to the events listed above, a Lane Adapter that is not the Upstream Adapter shall enter this state on any of the following events: Adapter receives an LT_Fall Transaction.
<b>4.2.1.2.2 Behavior in State</b>		
4.2.1.2.2#1	NT	A Lane Adapter that enters this state due to a disconnect shall enter Lane Initialization starting from Phase 1.
4.2.1.2.2#2	TD 4.007	A Lane Adapter that enters this state from the Disabled State performs Lane Initialization after the Lane is enabled. The Lane Adapter shall start Lane Initialization from Phase 4. The USB4 Port shall maintain any state acquired in Phases 1 through 3 of previous Lane Initialization.
4.2.1.2.2#3	NT	A Lane Adapter that enters this state due to the Router entering Sleep state performs Lane Initialization after a Wake event. The Lane Adapter shall start Lane Initialization from Phase 2.

4.2.1.2.2#4	TD 4.033	A Lane Adapter that enters this state due to Link training timeout shall perform Lane Initialization starting from Phase 1
4.2.1.2.2#5	NT	Deprecated.
4.2.1.2.2#6	NT	Deprecated.
4.2.1.2.2#7	NT	Deprecated.
<b>4.2.1.2.3 Exit from State</b>		
4.2.1.2.3#1	NT	A Lane Adapter shall exit this state when the Lane's High-Speed transmitter is transmitting (completion of Phase 4 of Lane Initialization) and its receiver is enabled.
4.2.1.2.3#2	TD 4.009	After exiting the CLd state, a Lane Adapter shall transition to the Training.LOCK1 state.
<b>4.2.1.3 Training</b>		
<b>4.2.1.3.1 Entry to State</b>		
4.2.1.3.1#1	NT	A Lane Adapter shall enter this state on any of the following events: After exiting the CLd state.
4.2.1.3.1#2	TD 4.040 TD 4.041	A Lane Adapter shall enter this state on any of the following events: When recovering from a USB4 Link error.
4.2.1.3.1#3	TD 4.010 TD 4.011 TD 4.012 TD 4.013	A Lane Adapter shall enter this state on any of the following events: After exiting the CL2 or CL1 states.
<b>4.2.1.3.2 Behavior in State</b>		
4.2.1.3.2#1	TD 4.009 TD 4.032 TD 4.033	A Lane Adapter shall follow the Training Sub-state machine described in Figure 4-9 with the behavior described in Table 4-19 and the sub-state transitions described in Table 4-20.
4.2.1.3.2#2	NT	If the transition to Training state is from CLx state, the sub-state transitions shall occur within tTrainingTransition time from receiving the last bit of the relevant Symbols.
4.2.1.3.2#3	NT	In LOCK1 state, a transmitter shall send back-to-back SLOS1.
4.2.1.3.2#4	NT	In LOCK2 state, a transmitter shall send back-to-back SLOS2.
4.2.1.3.2#5	NT	In TS1 state, a transmitter send back-to-back TS1 Ordered Sets.

4.2.1.3.2#6	NT	In TS2 state, a transmitter send back-to-back TS2 Ordered Sets.
<b>4.2.1.3.3 Exit from State</b>		
4.2.1.3.3#1	TD 4.009	A Lane Adapter that transitions from CLd state to Training state shall complete training and transition to the CL0 state within tTrainingAbort1 after entering the Training state.
4.2.1.3.3#2	NT	If the Adapter does not transition to CL0 state within tTrainingAbort1, the Router shall initiate a Disconnect by driving SBTX to a logical low state for tDisconnectTx.
4.2.1.3.3#3	TD 4.040	A Lane Adapter that transitions from a state other than CLd to Training state shall complete training and transition to the CL0 state within tTrainingAbort2 after entering the Training state.
4.2.1.3.3#4	TD 4.033	If the Adapter does not transition to CL0 state within tTrainingAbort2, the Router shall initiate a Disconnect by driving SBTX to a logical low state for tDisconnectTx.
4.2.1.3.3#5	TD 4.006	A Hot Plug Event Packet shall be sent on transition to CL0 state if the Adapter is part of a Downstream Facing Port and it entered Training state from a CLd state.
4.2.1.3.3#6	TD 4.009	A Lane Adapter shall set the Plugged bit to 1b when it transitions from the Training state to the CL0 state.
<b>4.2.1.3.4 SLOS1 and SLOS2</b>		
4.2.1.3.4#1	IOP	When operating in Gen 2 mode with RS-FEC encoding disabled, SLOS shall be encoded using 64b/66b encoding.
4.2.1.3.4#2	IOP	When operating in Gen 2 mode with RS-FEC encoding enabled, SLOS that are not RS-FEC encoded shall be encoded using 128b/132b encoding.
4.2.1.3.4#3	IOP	When operating in Gen 3 mode, SLOS that are not RS-FEC encoded shall be encoded using 128b/132b encoding.
4.2.1.3.4#4	IOP	The SLOS1 and SLOS2 shall not be scrambled, and the scrambler shall not advance upon receive/transmit.
4.2.1.3.4#5	TD 4.009	When transmitting SLOS1 or SLOS2 using 64b/66b encoding, a Router shall transmit all 32 SLOS Symbols in their entirety.
4.2.1.3.4#6	TD 4.009	When using 128b/132b encoding, a Router shall transmit all 16 SLOS Symbols in their entirety.
4.2.1.3.4#7	NT	A Router shall not transmit an incomplete SLOS.

<b>4.2.1.3.5 TS1 and TS2 Ordered Sets</b>		
4.2.1.3.5#1	NT	A TS1 Ordered Set and a TS2 Ordered Set shall have the structure in Table 4-25.
4.2.1.3.5#2	TD 4.036	Bits 63:59 (Rsvd) of a TS1 or TS2 Ordered Set shall be ignored by a receiver.
4.2.1.3.5#3	TD 4.009	Bits 58:56 (Lane Bonding Target) of a TS1 or TS2 Ordered Set shall be set according to the value of the Target Link Width field of the USB4 Adapter Configuration Capability: 000b – Establish two single-Lane Links and 001b – Establish a dual-lane Link. All other values are reserved and shall not be used.
4.2.1.3.5#4	TD 4.009	Bits 55:48 (Lane Number) of a TS1 or TS2 Ordered Set shall be set to match the Lane number: 00h - Lane 0 and 01h - Lane 1. All other values are reserved and shall not be used.
4.2.1.3.5#5	TD 4.009 TD 4.036	Bits 47:32 (Rsvd) of a TS1 or TS2 Ordered Set shall be ignored by a receiver.
4.2.1.3.5#6	BC	Bits 31:29 (Rsvd) of a TS1 or TS2 Ordered Set shall be set to 0 by a transmitter.
4.2.1.3.5#7	TD 4.036	Bits 31:29 (Rsvd) of a TS1 or TS2 Ordered Set shall be ignored by a receiver.
4.2.1.3.5#8	TD 4.009	A Transmitter shall set bits 28:26 (Lane Bonding Target 2) of a TS1 or TS2 Ordered Set to match the Lane Bonding Target field.
4.2.1.3.5#9	TD 4.036	Bits 28:26 (Lane Bonding Target 2) of a TS1 or TS2 Ordered Set shall be ignored by a receiver.
4.2.1.3.5#10	TD 4.036	Bits 25:16 (Rsvd) of a TS1 or TS2 Ordered Set shall be ignored by a receiver.
4.2.1.3.5#11	TD 4.009	Bits 9:0 (SCR) of a TS1 or TS2 Ordered Set shall be set to 00 1111 0010b to indicate that Ordered Set contents are scrambled.
<b>4.2.1.4 CL0</b>		
<b>4.2.1.4.1 Entry to State</b>		
4.2.1.4.1#1	TD 4.005 TD 4.009	A Lane Adapter shall enter this state upon any of the following events: Successful completion of Lane training.
4.2.1.4.1#2	TD 4.009	A Lane Adapter shall enter this state upon any of the following events: Successful completion of Lane Bonding.
4.2.1.4.1#3	TD 4.014 TD 4.015	A Lane Adapter shall enter this state upon any of the following events: Exit from CL0s state

4.2.1.4.2 Behavior in State		
4.2.1.4.3 Exit from State		
4.2.1.4.3#1	NT	A Lane Adapter shall exit this state after one of the following occurs: Adapter Disable.
4.2.1.4.3#2	NT	A Lane Adapter that exits this state due to an Adapter disable shall transition to either the Disabled state or the CLd state as defined in Section 4.4.6.
4.2.1.4.3#3	NT	A Lane Adapter shall exit this state after one of the following occurs: Adapter disconnect. An Adapter that exits this state due to a disconnect event shall transition to the CLd state.
4.2.1.4.3#4	NT	A Lane Adapter shall exit this state after one of the following occurs: Reception of an LT_Fall Transaction. The Adapter shall transition to the CLd state.
4.2.1.4.3#5	TD 4.040 TD 4.041	A Lane Adapter shall exit this state after one of the following occurs: Transition to Training state when: An error event occurs that transitions the Lane Adapter to the Training.LOCK1 state.
4.2.1.4.3#6	TD 4.032 TD 4.033	A Lane Adapter shall exit this state after one of the following occurs: Transition to Training state when: Reception of any 2 SLOS Symbols in a row transitions the Lane Adapter either to the Training.LOCK1 sub-state or to the Training.LOCK2 sub-state.
4.2.1.4.3#7	NT	A Lane Adapter shall exit this state after one of the following occurs: Transition to CL0s, CL1, or CL2 states.
4.2.1.4.3#8	TD 4.009 TD 4.010 TD 4.011 TD 4.014 TD 4.015	A Lane Adapter shall exit this state after one of the following occurs: Transition to Lane Bonding state when either: The <i>Lane Bonding</i> bit in the USB4 Adapter Configuration Capability Register of either Adapter in the USB4 Port is set to 1b.
4.2.1.4.3#9	TD 4.010	A Lane Adapter shall exit this state after one of the following occurs: Transition to Lane Bonding state when either: 3 TS1 Ordered Sets are received in a row.
4.2.1.4.3#10	NT	A Lane Adapter shall not exit this state to enter Lane Bonding state while it is sending a Transport Layer Packet.
4.2.1.4.3#11	NT	The Adapter shall complete sending the packet before entering Lane Bonding state.

<b>4.2.1.5 Lane Bonding</b>		
<b>4.2.1.5.1 Entry to State</b>		
4.2.1.5.1#1	TD 4.009	A Lane Adapter shall enter this state from CL0 state on any of the following events: The Lane Bonding bit in the Lane Adapter Capability Register of either Adapter in the USB4 Port is set to 1b.
4.2.1.5.1#2	TD 4.009	An Adapter shall enter this state from CL0 state on any of the following events: Three TS1 Ordered Sets are received in a row.
<b>4.2.1.5.2 Behavior in State</b>		
4.2.1.5.2#1	TD 4.009 TD 4.034	A Lane Adapter shall follow the Lane Bonding sub-state machine described in Figure 4-10 with the behavior described in Table 4-26 and the state transitions described in Table 4-27.
4.2.1.5.2#2	NT	In TS1 state, transmitter shall send back-to-back TS1 Ordered Sets.
4.2.1.5.2#3	NT	In TS2 state, transmitter shall send back-to-back TS2 Ordered Sets.
<b>4.2.1.5.3 Exit from State</b>		
4.2.1.5.3#1	TD 4.009	A Lane Adapter shall exit this state as defined in Table 4-27.
4.2.1.5.3#2	TD 4.009	A Lane Adapter that exits this state due to successful completion shall transition to the CL0 state.
4.2.1.5.3#3	TD 4.009	A Lane Adapter that transitions to CL0 state shall continue sending TS2 Ordered Sets until the other Adapter enters CL0 state.
4.2.1.5.3#4	NT	A Lane Adapter that exits this state due to unsuccessful completion (i.e. Transitions 2, 4, and 5 in Table 4-27) shall transition to the Training.LOCK2 sub-state
<b>4.2.1.6 Low Power (CL0s, CL1, CL2)</b>		
4.2.1.6#1	NT	When a Lane Adapter supports CLx states, it shall enter or reject a CLx state as described in Section 4.2.1.6.2.
4.2.1.6#2	NT	When a Lane Adapter does not support CLx states, it shall reject entry to CLx state as described in Section 4.2.1.6.2.
<b>4.2.1.6.1 Ordered Sets</b>		
4.2.1.6.1#1	NT	Bits 9:0 (SCR) in a CL2_REQ Ordered Set payload shall be set to 00 1111 0010b to indicate that the Ordered Set contents are scrambled.
4.2.1.6.1#2	NT	Bits 9:0 (SCR) in a CL1_REQ Ordered Set payload shall be set to 00 1111 0010b to indicate that the Ordered Set contents are scrambled.



4.2.1.6.1#3	TD 4.010 TD 4.011	Bits 9:0 (SCR) in a CL2_ACK Ordered Set payload shall be set to 00 1111 0010b to indicate that the Ordered Set contents are scrambled.
4.2.1.6.1#4	TD 4.012 TD 4.013	Bits 9:0 (SCR) in a CL1_ACK Ordered Set payload shall be set to 00 1111 0010b to indicate that the Ordered Set contents are scrambled.
4.2.1.6.1#5	TD 4.014 TD 4.015	Bits 9:0 (SCR) in a CL0s_ACK Ordered Set payload shall be set to 00 1111 0010b to indicate that the Ordered Set contents are scrambled.
4.2.1.6.1#6	TD 4.010 TD 4.011 TD 4.012 TD 4.013	Bits 9:0 (SCR) in a CL_NACK Ordered Set payload shall be set to 00 1111 0010b to indicate that the Ordered Set contents are scrambled.
4.2.1.6.1#7	NT	Bits 9:0 (SCR) in a CL_OFF Ordered Set payload shall be set to 00 1111 0010b to indicate that the Ordered Set contents are scrambled.
<b>4.2.1.6.1.1 CL_WAKE1.X Ordered Sets</b>		
4.2.1.6.1.1#1	NT	A CL_WAKE1.X Ordered Set shall not be scrambled, and the scrambler shall not advance upon receive/transmit.
4.2.1.6.1.1#2	NT	Unless otherwise mentioned, a CL_WAKE1.X Ordered Set shall be transmitted in its entirety.
<b>4.2.1.6.1.2 CL_WAKE2.X Ordered Sets</b>		
4.2.1.6.1.2#1	NT	When operating in Gen 2 mode with RS-FEC encoding disabled, a CL_WAKE2.X Ordered Set has the structure of an SLOS2 with 64/66b encoding and the following modifications: Bits [63:56] of an even numbered Symbol payload shall be CXh, where “X” is the hexadecimal index from the last CL_WAKE1.X Ordered Set received.
4.2.1.6.1.2#2	NT	When operating in Gen 2 mode with RS-FEC encoding disabled, a CL_WAKE2.X Ordered Set has the structure of an SLOS2 with 64/66b encoding and the following modifications: Bits [63:56] of an odd numbered Symbol payload shall be the logical inverse of CXh, where "X" is the hexadecimal index from the last CL_WAKE1.X Ordered Set received.
4.2.1.6.1.2#3	NT	When operating in Gen 2 mode and RS-FEC encoding is enabled, a CL_WAKE2.X Ordered Set has the structure of an SLOS2 with 128b/132b Encoding and the following modifications: Bits [127:120] of an even numbered Symbol payload shall be CXh, where “X” is the hexadecimal index from the last CL_WAKE1.X Ordered Set received.

4.2.1.6.1.2#4	NT	When operating in Gen 2 mode and RS-FEC encoding is enabled, a CL_WAKE2.X Ordered Set has the structure of an SLOS2 with 128b/132b Encoding and the following modifications: Bits [63:56] of an even numbered Symbol payload shall be CXh, where “X” is the hexadecimal index from the last CL_WAKE1.X Ordered Set received.
4.2.1.6.1.2#5	NT	When operating in Gen 2 mode and RS-FEC encoding is enabled, a CL_WAKE2.X Ordered Set has the structure of an SLOS2 with 128b/132b Encoding and the following modifications: Bits [127:120] of an odd numbered Symbol payload shall be the logical inverse of CXh, where “X” is the hexadecimal index from the last CL_WAKE1.X Ordered Set received.
4.2.1.6.1.2#6	NT	When operating in Gen 2 mode and RS-FEC encoding is enabled, a CL_WAKE2.X Ordered Set has the structure of an SLOS2 with 128b/132b Encoding and the following modifications: Bits [63:56] of an odd numbered Symbol payload shall be the logical inverse of CXh, where “X” is the hexadecimal index from the last CL_WAKE1.X Ordered Set received.
4.2.1.6.1.2#7	NT	When operating in Gen 3 mode, a CL_WAKE2.X Ordered Set has the structure of an SLOS2 with 128b/132b Encoding and the following modifications: Bits [127:120] of an even numbered Symbol payload shall be CXh, where “X” is the hexadecimal index from the last CL_WAKE1.X Ordered Set received.
4.2.1.6.1.2#8	NT	When operating in Gen 3 mode, a CL_WAKE2.X Ordered Set has the structure of an SLOS2 with 128b/132b Encoding and the following modifications: Bits [127:120] of an odd numbered Symbol payload shall be the logical inverse of CXh, where “X” is the hexadecimal index from the last CL_WAKE1.X Ordered Set received.
4.2.1.6.1.2#9	TD 4.011 TD 4.013	A CL_WAKE2.X Ordered Set shall not be scrambled, and the scrambler shall not advance upon receive/transmit.
4.2.1.6.1.2#10	TD 4.011 TD 4.013	Unless otherwise mentioned, a CL_WAKE2.X Ordered Set shall be transmitted in its entirety.
<b>4.2.1.6.2 Entry to State</b>		
4.2.1.6.2#1	TD 4.010 TD 4.011 TD 4.012 TD 4.013	(Requesting Port) The request Ordered Set shall be sent back-to-back until a response Ordered Set is received from the Link Partner.
4.2.1.6.2#2	NT	(Requesting Port) An Adapter shall send CL2_REQ Ordered Sets when its USB4 Port does not assert any objections to enter CL2 state.
4.2.1.6.2#3	NT	(Requesting Port) An Adapter shall send CL1_REQ Ordered Sets when its USB4 Port asserts an objection to enter CL2 state but does not assert any objections to enter CL1 state.

4.2.1.6.2#4	NT	(Requesting Port) If a Lane Adapter receives a CL1_REQ Ordered Set or a CL2_REQ Ordered Set from its Link Partner, it shall not request entry to a Low Power state until after transitioning back to CL0.
4.2.1.6.2#5	NT	(Requesting Port) If the Requesting Port asserts an objection after the Lane Adapter has sent a request Ordered Set, the Lane Adapter shall ignore the objection until the Lane Adapter is either in a CLx state or receives a CL_NACK Ordered Set.
4.2.1.6.2#6	NT	(Responding Port) A Lane Adapter shall reject a request to enter a Low Power state when all of the following are true: The Adapter has already sent a request to enter the same low power state; and The <i>PM Secondary</i> bit in the Lane 0 Adapter and/or the Lane 1 Adapter of the Responding Port is set to 0b.
4.2.1.6.2#7	TD 4.010 TD 4.011 TD 4.012 TD 4.013	The Lane Adapter shall send CL_NACK Ordered Sets for as long as it receives the request Ordered Set from the Link Partner.
4.2.1.6.2#8	NT	A Lane Adapter that receives a CL1_REQ Ordered Set after it has sent a CL2_REQ Ordered Set, shall accept the request by responding with CL1_ACK Ordered Sets. The Adapter shall stop sending CL2_REQ Ordered Sets.
4.2.1.6.2#9	NT	A Lane Adapter that receives a CL2_REQ Ordered Set after it has sent a CL1_REQ Ordered Set, shall not respond to the request and shall continue sending CL1_REQ Ordered Sets.
4.2.1.6.2#10	TD 4.010 TD 4.011	Else, if the Responding Port does not assert an objection to enter CL2 state, it shall respond to CL2_REQ Ordered Sets with a CL2_ACK Ordered Set.
4.2.1.6.2#11	TD 4.012 TD 4.013	Else, if the Responding Port does not assert an objection to enter CL1 state, it shall respond to CL2_REQ or CL1_REQ Ordered Sets with a CL1_ACK Ordered Set.
4.2.1.6.2#12	TD 4.014 TD 4.015	Else, if the <i>CL0s Enable</i> bit is set to 1b in the Lane 0 Adapter of the Responding Port and the Responding Port can meet the timing of both <i>tCL0sEntry</i> and <i>tCL0sExit</i> , a Lane Adapter shall respond to a request to enter a Low Power state with a CL0s_ACK Ordered Set. The CL0s_ACK Ordered Set shall be sent 16 times.
4.2.1.6.2#13	TD 4.010 TD 4.011 TD 4.012 TD 4.013	Else, a Lane Adapter shall respond to a request to enter a Low Power state with CL_NACK Ordered Sets within a time which is lesser than ( <i>tCL0sEntry</i> + <i>tCL0sExit</i> ). The CL_NACK Ordered Sets shall be sent 16 times.

4.2.1.6.2#14	TD 4.010 TD 4.011 TD 4.012 TD 4.013	The Adapter shall resume regular CL0 operation in the transmit direction once it stops sending the CL_NACK Ordered Sets.
4.2.1.6.2#15	NT	If the Responding Port asserts an objection after the Lane Adapter has sent a CLx_ACK response Ordered Set, but before the transition to CLx state is complete, the Lane Adapter shall ignore the objection until it transitions to the CLx state.
4.2.1.6.2#16	NT	A Lane Adapter shall stop sending a request to enter a Low Power state when it receives a response Ordered Set from the Link Partner.
4.2.1.6.2#17	TD 4.010 TD 4.011 TD 4.012 TD 4.013	(Requesting Port) If the response is a CL2_ACK, a CL1_ACK, or a CL0s_ACK Ordered Set, the Lane Adapter shall send 375 CL_OFF Ordered Sets. The CL_OFF Ordered sets shall be sent back-to-back.
4.2.1.6.2#18	TD 4.010 TD 4.011 TD 4.012 TD 4.013	(Requesting Port) The first CL_OFF Ordered Set shall be sent within tCLxResponse after detection of the response.
4.2.1.6.2#19	NT	(Requesting Port) If the response is a CL2_ACK or a CL1_ACK Ordered Set, the Adapter shall also shut down its receiver.
4.2.1.6.2#20	TD 4.010 TD 4.011 TD 4.012 TD 4.013	(Requesting Port) If the response is a CL_NACK Ordered Set, the Adapter shall not send another CL2_REQ Ordered Set or CL1_REQ Ordered Set for tCLxRetry after receiving the CL_NACK Ordered Set.
4.2.1.6.2#21	TD 4.010 TD 4.011 TD 4.012 TD 4.013	(Requesting Port) If the response is a CL_NACK Ordered Set, all Lane Adapters in the Requesting Port shall resume regular CL0 operation.
4.2.1.6.2#22	NT	If the Requesting Port detects Link errors in the direction of the Link Partner before receiving a response Ordered Set from the Link Partner, it shall: Stop sending the request to enter a Low Power state.
4.2.1.6.2#23	NT	If the Requesting Port detects Link errors in the direction of the Link Partner before receiving a response Ordered Set from the Link Partner, it shall: Transition its Lane Adapters to the Training.LOCK1 sub-state and send the first SLOS within tCLxResponse of detecting the Link error.

4.2.1.6.2#24	NT	In the Requesting Port, a Lane Adapter shall do the following after sending 375 CL_OFF Ordered Sets: 1. Shut down its transmitter within tTxOff time.
4.2.1.6.2#25	TD 4.010 TD 4.011	In the Requesting Port, a Lane Adapter shall do the following after sending 375 CL_OFF Ordered Sets: 2. Transition state as follows: If the response from the Link Partner was CL2_ACK, transition to CL2 state.
4.2.1.6.2#26	TD 4.012 TD 4.013	In the Requesting Port, a Lane Adapter shall do the following after sending 375 CL_OFF Ordered Sets: 2. Transition state as follows: If the response from the Link Partner was CL1_ACK, transition to CL1 state.
4.2.1.6.2#27	NT	In the Requesting Port, a Lane Adapter shall do the following after sending 375 CL_OFF Ordered Sets: 2. Transition state as follows: If the response from the Link Partner was CL0s_ACK, transition to CL0s state.
4.2.1.6.2#28	NT	In the Requesting Port, a Lane Adapter shall do the following after sending 375 CL_OFF Ordered Sets: 3. Enable exit from CLx state as follows: If the response from the Link Partner was CL2_ACK or CL1_ACK, wait tEnterLFPS1 time after the state transition in Step 2), then enable transmission and detection of Low Frequency Periodic Signaling (LFPS).
4.2.1.6.2#29	NT	In the Requesting Port, a Lane Adapter shall do the following after sending 375 CL_OFF Ordered Sets: 3. Enable exit from CLx state as follows: If the response from the Link Partner was CL0s_ACK, wait tEnterLFPS4 time after the state transition in Step 2), then enable transmission of Low Frequency Periodic Signaling (LFPS).
4.2.1.6.2#30	TD 4.010 TD 4.011 TD 4.012 TD 4.013 TD 4.014 TD 4.015	In the Responding Port, a Lane Adapter shall shut down its receiver after receiving a CL_OFF Ordered Set. If the Adapter sent CL0s_ACK Ordered Sets, it shall also transition to the CL0s state.
4.2.1.6.2#31	NT	In the Responding Port, The Adapter shall then enable exit from the Low Power state as follows: If the Adapter sent CL2_ACK or CL1_ACK, wait tEnterLFPS2 time after shutting down the receiver, then enable transmission and detection of Low Frequency Periodic Signaling (LFPS).
4.2.1.6.2#32	NT	In the Responding Port, The Adapter shall then enable exit from the Low Power state as follows: If the Adapter sent CL0s_ACK, wait tEnterLFPS5, then enable detection of Low Frequency Periodic Signaling (LFPS).
4.2.1.6.2#33	NT NT	Deprecated.

4.2.1.6.2#34	NT NT	Deprecated.
4.2.1.6.2#35	NT	Deprecated.
4.2.1.6.2#36	NT	Deprecated.
4.2.1.6.2#37	NT	Deprecated.
4.2.1.6.2#38	TD 4.037	A Lane Adapter may transition to Training.LOCK1 sub-state as a result of Logical Layer errors during the entry to Low Power state with the following exceptions: After sending the first CL2_ACK, CL1_ACK, or CL0s_ACK Ordered Set, a Lane Adapter shall not enter Training state as a result of Logical Layer errors in its receivers.
4.2.1.6.2#39	NT	A Lane Adapter may transition to Training.LOCK1 sub-state as a result of Logical Layer errors during the entry to Low Power state with the following exceptions: A Lane Adapter that is sending CL_OFF Ordered Sets shall complete the transition to CL2, CL1, or CL0s state.
4.2.1.6.2#40	NT	After sending a CL_NACK Ordered Set, a port shall be able to meet tCL0sEntry and tCL0sExit requirements within tCLxSetup, and shall keep meeting these timing requirements for a duration of tCLxAccept.
<b>4.2.1.6.3 Objections</b>		
4.2.1.6.3#1	TD 4.010 TD 4.011	A USB4 Port shall assert an objection to enter CL2 state if: The <i>CL2 Support</i> bit in the Lane 0 Adapter is 0.
4.2.1.6.3#2	NT	A USB4 Port shall assert an objection to enter CL2 state if: The <i>CL2 Enable</i> bit in the Lane 0 Adapter is 0b.
4.2.1.6.3#3	NT	A USB4 Port shall assert an objection to enter CL2 state if: There is a Transport Layer Packet to be sent over the USB4 Port.
4.2.1.6.3#4	NT	A USB4 Port shall assert an objection to enter CL2 state if: The Lane 0 Adapter is referenced in an <i>Egress Adapter</i> field of a PCIe Adapter's Routing Table and the PCIe Adapter is not in PCIe L1 state.
4.2.1.6.3#5	NT	A USB4 Port shall assert an objection to enter CL2 state if: The Lane 0 Adapter is referenced in an <i>Egress Adapter</i> field of the Upstream PCIe Adapter's Routing Table, and either the No-Snoop Latency value or the Snoop Latency value in the last LTR Message transmitted upstream is smaller than the sum of the CL2 entry and exit latency.
4.2.1.6.3#6	NT	A USB4 Port shall assert an objection to enter CL2 state if: The Lane 0 Adapter is referenced in an <i>Egress Adapter</i> field of a Downstream PCIe Adapter's Routing Table, and either the No-Snoop Latency value or the Snoop Latency value in the last LTR Message received by the Downstream PCIe Adapter is smaller than the sum of the CL2 entry and exit latency.

4.2.1.6.3#7	NT	A USB4 Port shall assert an objection to enter CL2 state if: The Lane 0 Adapter is referenced in an <i>Egress Adapter</i> field of a DP IN Adapter's Routing Table.
4.2.1.6.3#8	NT	A USB4 Port shall assert an objection to enter CL2 state if: The Lane 0 Adapter is referenced in an <i>Egress Adapter</i> field of a DP OUT Adapter's Routing Table and a Packet is issued from the DP OUT Adapter.
4.2.1.6.3#9	NT	A USB4 Port shall assert an objection to enter CL2 state if: The Lane 0 Adapter is referenced in an <i>Egress Adapter</i> field of a USB3 Adapter's Routing Table and the USB3 link between the USB3 Adapter and the internal USB3 device is not in U2 or U3 state.
4.2.1.6.3#10	NT	A USB4 Port shall assert an objection to enter CL2 state if: The Lane 0 Adapter is referenced in an <i>Egress Adapter</i> field of a USB3 Adapter's Routing Table, the USB3 link between the USB3 Adapter and the internal USB3 device is in U2 state, and CL2 entry is disabled in U2 state.
4.2.1.6.3#11	NT	A USB4 Port shall assert an objection to enter CL2 state if: The Lane 0 Adapter is referenced in an <i>Egress Adapter</i> field of a USB3 Adapter's Routing Table, the USB3 link between the USB3 Adapter and the internal USB3 device is in U3 state, and CL2 entry is disabled in U3 state.
4.2.1.6.3#12	NT	A USB4 Port shall assert an objection to enter CL2 state if: Entry to CL2 state would delay a pending Time Sync handshake. This objection shall be asserted until the Time Sync handshake is complete.
4.2.1.6.3#13	NT	(Host Routers Only) A USB4 Port shall assert an objection to enter CL2 state if: The Lane 0 Adapter is referenced in an <i>Egress Adapter</i> field of a Host Interface Adapter's Routing Table, whose Path corresponds to a Transmit Descriptor Ring that disables CL2 entry.
4.2.1.6.3#14	NT	(Host Routers Only) A USB4 Port shall assert an objection to enter CL2 state if: The Lane 0 Adapter is referenced in an <i>Egress Adapter</i> field of a Host Interface Adapter's Routing Table and the Host Interface has a Packet to send over the Adapter.
4.2.1.6.3#15	NT	(Device Routers Only) One of its Ports is in the process of CL0s, CL1 or CL2 exit flow.
4.2.1.6.3#16	TD 4.012 TD 4.013	A USB4 Port shall assert an objection to enter CL1 state if: The <i>CL1 Support</i> bit in the Lane 0 Adapter is 0b.
4.2.1.6.3#17	NT	A USB4 Port shall assert an objection to enter CL1 state if: The <i>CL1 Enable</i> bit in the Lane 0 Adapter is 0b.
4.2.1.6.3#18	NT	A USB4 Port shall assert an objection to enter CL1 state if: There is a Transport Layer Packet to be sent over the USB4 Port.

4.2.1.6.3#19	NT	A USB4 Port shall assert an objection to enter CL1 state if: The Lane 0 Adapter is referenced in an <i>Egress Adapter</i> field of a PCIe Adapter's Routing Table and the PCIe Adapter is not in PCIe L1 state.
4.2.1.6.3#20	NT	A USB4 Port shall assert an objection to enter CL1 state if: The Lane 0 Adapter is referenced in an <i>Egress Adapter</i> field of the Upstream PCIe Adapter's Routing Table, and either the No-Snoop Latency value or the Snoop Latency value in the last LTR Message transmitted upstream is smaller than the sum of the CL1 entry and exit latency.
4.2.1.6.3#21	NT	A USB4 Port shall assert an objection to enter CL1 state if: The Lane 0 Adapter is referenced in an <i>Egress Adapter</i> field of a Downstream PCIe Adapter's Routing Table, and either the No-Snoop Latency value or the Snoop Latency value in the last LTR Message received by the Downstream PCIe Adapter is smaller than the sum of the CL1 entry and exit latency.
4.2.1.6.3#22	NT	A USB4 Port shall assert an objection to enter CL1 state if: The Lane 0 Adapter is referenced in an <i>Egress Adapter</i> field of a DP IN Adapter's Routing Table.
4.2.1.6.3#23	NT	A USB4 Port shall assert an objection to enter CL1 state if: The Lane 0 Adapter is referenced in an <i>Egress Adapter</i> field of a DP OUT Adapter's Routing Table and a Packet is issued from the DP OUT Adapter.
4.2.1.6.3#24	NT	A USB4 Port shall assert an objection to enter CL1 state if: The Lane 0 Adapter is referenced in an <i>Egress Adapter</i> field of a USB3 Adapter's Routing Table and the USB3 link between the USB3 Adapter and the internal USB3 device is not in U2 or U3 state.
4.2.1.6.3#25	NT	A USB4 Port shall assert an objection to enter CL1 state if: The Lane 0 Adapter is referenced in an <i>Egress Adapter</i> field of a USB3 Adapter's Routing Table, the USB3 link between the USB3 Adapter and the internal USB3 device is in U3 state, and CL1 entry is disabled in USB U3 state.
4.2.1.6.3#26	NT	A USB4 Port shall assert an objection to enter CL1 state if: The Lane 0 Adapter is referenced in an <i>Egress Adapter</i> field of a USB3 Adapter's Routing Table, the USB3 Adapter is in USB U3 state, and CL1 entry is disabled in USB U3 state.
4.2.1.6.3#27	NT	A USB4 Port shall assert an objection to enter CL1 state if: Entry to CL1 state would delay a pending Time Sync handshake.
4.2.1.6.3#28	NT	(Host Routers Only) A USB4 Port shall assert an objection to enter CL1 state if: The Lane 0 Adapter is referenced in an <i>Egress Adapter</i> field of a Host Interface Adapter's Routing Table, whose Path corresponds to a Transmit Descriptor Ring that disables CL1 entry.
4.2.1.6.3#29	NT	(Host Routers Only) A USB4 Port shall assert an objection to enter CL1 state if: The Lane 0 Adapter is referenced in an <i>Egress Adapter</i> field of a Host Interface Adapter's Routing Table and the Host Interface has a Packet to send over the Adapter.



4.2.1.6.3#30	NT	(Device Routers Only) One of its Ports is in the process of CL0s, CL1 or CL2 exit flow.
<b>4.2.1.6.4 Behavior in State</b>		
4.2.1.6.4#1	NT	While in CL2 state, the transmitter shall be in electrical idle. Lane common mode voltages shall be maintained.
4.2.1.6.4#2	TD 4.012 TD 4.013	While in CL1 state, the transmitter shall be in electrical idle. Lane common mode voltages shall be maintained.
4.2.1.6.4#3	TD 4.014 TD 4.015	While in CL0s state, the transmitter at the requesting USB4 Port shall be in electrical idle. Lane common mode voltages shall be maintained.
4.2.1.6.4#4	NT	Receiver termination shall be maintained in CL0s CL1, and CL2 states.
<b>4.2.1.6.5 Exit from State</b>		
4.2.1.6.5#1	TD 4.016	A Lane Adapter shall initiate transition out of CL2, CL1, or CL0s state when: An objection is set in the USB4 Port that would have prevented the Adapter from entering the low power state.
4.2.1.6.5#2	NT	A Lane Adapter shall initiate transition out of CL2, CL1, or CL0s state when: The Adapter is in CL0s state and a CL2_REQ Ordered Set or a CL1_REQ Ordered Set is received from the Link Partner.
4.2.1.6.5#3	NT	A Lane Adapter shall initiate transition out of CL2, CL1, or CL0s state when: The Adapter is in CL0s state and it detects Link errors that cause the Adapter to transition to Training state.
4.2.1.6.5#4	NT	A Lane Adapter shall initiate transition out of CL2, CL1, or CL0s state when: The Adapter is in a CL1 state or a CL2 state and it is referenced in an <i>Egress Adapter</i> field of a Lane Adapter's Routing Table and the other Adapter's receiver is exiting from CL0s, CL1, or CL2 states.
4.2.1.6.5#5	NT	A Lane Adapter shall initiate transition out of CL2, CL1, or CL0s state when: The Adapter is in CL0s state and it is referenced in an <i>Egress Adapter</i> field of a Lane Adapter's Routing Table and the other Adapter's receiver is exiting from CL0s, CL1, or CL2 states.
<b>4.2.1.6.5.1 Exit Flow from CL0s State</b>		
4.2.1.6.5.1#1	TD 4.014 TD 4.015 TD 4.016	The USB4 Port initiating exit from CL0s state shall: 1. Send a Low Frequency Periodic Signaling (LFPS) burst on all Lanes for the duration of at least 16 LFPS cycles.
4.2.1.6.5.1#2	TD 4.016	The USB4 Port initiating exit from CL0s state shall: 2. Return to Electrical Idle for tPreData.

4.2.1.6.5.1#3	TD 4.016	The USB4 Port initiating exit from CL0s state shall: 3. Start transmitting SLOS1 on each Lane of the USB4 Port. Any received CL_WAKE Ordered Sets shall be ignored.
4.2.1.6.5.1#4	TD 4.016	The USB4 Port initiating exit from CL0s state shall: 4. On detection of 2 back-to-back TS2 Ordered Sets, stop sending SLOS1 and send at least 16 TS2 Ordered Sets.
4.2.1.6.5.1#5	TBD	The first TS2 Ordered Set shall be sent within tTrainingTransition after detection of the second TS2 Ordered Set.
4.2.1.6.5.1#6	NT	Before transmitting the first TS2 Ordered Sets: The scrambler shall load a new seed; Activate RS-FEC; Enable SSC if SSC is disabled.
4.2.1.6.5.1#7	TBD	If the receiver did not detect 2 back-to-back TS2 Ordered Sets within tTrainingAbort2 time after the transmitter started sending SLOS1 it shall initiate a Disconnect by driving SBTX to a logical low state for tDisconnectTx.
4.2.1.6.5.1#8	TD 4.016	The USB4 Port initiating exit from CL0s state shall: 5. Transition to CL0 state.
4.2.1.6.5.1#9	TD 4.016	If the USB4 Port operated as a Dual-Lane Link prior to entry to CL0s state, the USB4 Port shall resume operation as a Dual-Lane Link independent of the setting of the TS2 Ordered Sets. A de-skew Ordered Set shall be sent. The scrambler shall load a new seed.
4.2.1.6.5.1#10	NT	If the Router initiated exit from CL0s state due to receiving CL1_REQ or CL2_REQ Ordered Sets, then the Router shall not send any Transport Layer Packets before responding to the request Ordered Sets according to the rules in Section 4.2.1.6.2 or with CL_NACK. The Router shall resume regular CL0 operation once it stops sending CL_NACK Ordered Sets.
4.2.1.6.5.1#11	TD 4.014 TD 4.015	Upon detecting 2 LFPS cycles, a Lane Adapter in CL0s state shall: 1. Enable the receiver to start bit and symbol synchronization not earlier than tCLxIdleRx after the last LFPS cycle received. An Adapter shall complete Symbol lock within tWarmUpCL0s time from the reception of the first LFPS cycle.
4.2.1.6.5.1#12	TD 4.014 TD 4.015	Upon detecting 2 LFPS cycles, a Lane Adapter in CL0s state shall: 2. On reception of 3 back-to-back CL_WAKE1.X Ordered Set Symbols by the Lane 0 Adapter, transmit at least 8 CL_WAKE2.X Ordered Set Symbols on each enabled Lane of the USB4 Port.
4.2.1.6.5.1#13	TD 4.038	If 3 back-to-back CL_WAKE1.(X+1) Ordered Set Symbols or 3 back-to-back SLOS Symbols are not received within tCL0sSwitch time after receiving a CL_WAKE1.X Ordered Set Symbol, then the Adapter shall transition to the Training.LOCK1 sub-state.

4.2.1.6.5.1#14	NT	If the Router initiated exit from CL0s state by sending CL1_REQ or CL2_REQ Ordered Sets, then the Router shall continue sending the Ordered Sets instead of sending Transport Layer Packets. The Router shall not send any Transport Layer Packets after sending the first CL1_REQ or a CL2_REQ Ordered Set.
4.2.1.6.5.1#15	TD 4.014 TD 4.015	Upon detecting 2 LFPS cycles, a Lane Adapter in CL0s state shall: 3. On detection of 3 back-to-back SLOS Symbols by all enabled Adapters of the USB4 Port, transmit 16 TS2 Ordered Sets in each enabled Lane of the USB4 Port
4.2.1.6.5.1#16	TD 4.014 TD 4.015	Upon detecting 2 LFPS cycles, a Lane Adapter in CL0s state shall: 4. On detection of 2 back-to-back TS2 Ordered Sets, transition to CL0 state: If the Router initiated exit from CL0s state by sending CL1_REQ or CL2_REQ Ordered Sets, then the Router shall continue to send the Ordered Sets. The Router shall not send any Transport Layer Packets before completing the CLx entry flow.
4.2.1.6.5.1#17	TD 4.038	Upon detecting 2 LFPS cycles, a Lane Adapter in CL0s state shall: 4. On detection of 2 back-to-back TS2 Ordered Sets, transition to CL0 state: If the Adapter does not detect 2 back-to-back TS2 Ordered Sets in tTS2Timeout from transmitting TS2 Ordered Sets, the Lane Adapters in the Port shall enter the Training state.
4.2.1.6.5.1#18	TBD	In order to limit the CL0s exit time to 245μs, a Router shall comply with the following equation: $tWarmUpCL0s = 6 \times tWakeResponse + tTrainingTransition < 80 \mu s$ .
4.2.1.6.5.1#19	NT	If the Link is operating at Gen 2 speed, the Adapter may transmit a partial CL_WAKE2.X Ordered Set in order to send the required number of CL_WAKE2.X Ordered Set Symbols. Otherwise, the Wake Ordered Set shall be transmitted in its entirety.
<b>4.2.1.6.5.2 Exit Flow from CL1 or CL2 State (No Re-timers on the Link)</b>		
4.2.1.6.5.2#1	TD 4.016 TD 4.010 TD 4.012	The USB4 Port initiating exit from CL1 or CL2 state shall: 1. Send a Low Frequency Periodic Signaling (LFPS) burst on each Lane until the receiver detects LFPS.
4.2.1.6.5.2#2	TBD	If the receiver did not detect LFPS after tTrainingAbort2 time the Router shall initiate a Disconnect by driving SBTX to a logical low state for tDisconnectTx.
4.2.1.6.5.2#3	NT	The USB4 Port initiating exit from CL1 or CL2 state shall: 2. Return to Electrical Idle for tPreData.
4.2.1.6.5.2#4	TD 4.016 TD 4.010 TD 4.012	The USB4 Port initiating exit from CL1 or CL2 state shall: 3. Start transmitting SLOS1 on the Lane.

4.2.1.6.5.2#5	TD 4.016 TD 4.010 TD 4.012	The USB4 Port initiating exit from CL1 or CL2 state shall: 4. Enable the receiver to start bit and symbol synchronization not earlier than tCLxIdleRx after the last LFPS cycle received. A Lane Adapter shall complete Symbol lock within tRxLock time.
4.2.1.6.5.2#6	TD 4.016 TD 4.010 TD 4.012	The USB4 Port initiating exit from CL1 or CL2 state shall: 5. Transition the Lane Adapter to Training.LOCK1 sub-state.
4.2.1.6.5.2#7	NT	On transition to the TS1 sub-state, the USB4 Port shall enable SSC if SSC is disabled.
4.2.1.6.5.2#8	TD 4.010 TD 4.012	Upon detecting 2 LFPS cycles, a Lane Adapter in CL1 or CL2 state shall: 1. Send a Low Frequency Periodic Signaling (LFPS) burst on the Lane for the duration of at least 5 LFPS cycles and for no more than tLFPSDuration. If the Lane Adapter is in CL1 state, the first LFPS shall be sent within tWarmUpCL1 after receiving the first LFPS cycle. If the Lane Adapter is in CL2 state, the first LFPS shall be sent within tWarmUpCL2 after receiving the first LFPS cycle.
4.2.1.6.5.2#9	NT	Upon detecting 2 LFPS cycles, a Lane Adapter in CL1 or CL2 state shall: 2. Return to Electrical Idle for tPreData.
4.2.1.6.5.2#10	TD 4.010 TD 4.012	Upon detecting 2 LFPS cycles, a Lane Adapter in CL1 or CL2 state shall: 3. Start transmitting SLOS1 on the Lane.
4.2.1.6.5.2#11	TD 4.010 TD 4.012	Upon detecting 2 LFPS cycles, a Lane Adapter in CL1 or CL2 state shall: 4. Enable the receiver to start bit and symbol synchronization not earlier than tCLxIdleRx after the last LFPS cycle received. A Lane Adapter shall complete Symbol lock within tRxLock time.
4.2.1.6.5.2#12	TD 4.010 TD 4.012	Upon detecting 2 LFPS cycles, a Lane Adapter in CL1 or CL2 state shall: 5. Transition to Training.LOCK1 sub-state.
4.2.1.6.5.2#13	NT	On transition to the TS1 sub-state, the USB4 Port shall enable SSC if SSC is disabled
<b>4.2.1.6.5.3 Exit Flow from CL1 or CL2 State (Re-timers on the Link)</b>		
4.2.1.6.5.3#1	TD 4.016	The USB4 Port initiating exit from CL1 or CL2 state shall: 1. Send a Low Frequency Periodic Signaling (LFPS) burst on each Lane until its receiver detects LFPS.
4.2.1.6.5.3#2	TBD	If the receiver did not detect LFPS after tTrainingAbort2 time the Router shall initiate a Disconnect by driving SBTX to a logical low state for tDisconnectTx.
4.2.1.6.5.3#3	TD 4.016	The USB4 Port initiating exit from CL1 or CL2 state shall: 2. Return to Electrical Idle for tPreData.

4.2.1.6.5.3#4	TD 4.016	The USB4 Port initiating exit from CL1 or CL2 state shall: 3. Start transmitting SLOS1 on the Lane.
4.2.1.6.5.3#5	TD 4.016	The USB4 Port initiating exit from CL1 or CL2 state shall: 4. Enable the receiver to start bit and symbol synchronization not earlier than tCLxIdleRx after the last LFPS cycle received. A Lane Adapter shall complete Symbol lock within tRxLock time.
4.2.1.6.5.3#6	TD 4.016	The USB4 Port initiating exit from CL1 or CL2 state shall: 5. Upon reception of 3 back-to-back CL_WAKE1.X Ordered Set Symbols, start transmitting CL_WAKE2.X Ordered Set Symbols on the Lane. The Adapter shall ignore any received CL_WAKE2.Y (where Y is any value) Symbols interleaved with CL_WAKE1.X Ordered Set SymbolCL_WAKE1.X Ordered Set Symbols when it determines the reception of back-to-back CL_WAKE1.X Ordered Set SymbolCL_WAKE1.X Ordered Set Symbols.
4.2.1.6.5.3#7	TD 4.016	The USB4 Port initiating exit from CL1 or CL2 state shall: 6. Upon reception of 7 back-to-back CL_WAKE2.X Ordered Set Symbols or 7 back-to-back SLOS Symbols, transition the Adapter to Training.LOCK1 sub-state within tWakeResponse time.
4.2.1.6.5.3#8	NT	On transition to the TS1 sub-state, the USB4 Port shall enable SSC if SSC is disabled.
4.2.1.6.5.3#9	TD 4.011 TD 4.013	Upon detecting 2 LFPS cycles, a Lane Adapter in CL1 or CL2 state shall: 1. Send a Low Frequency Periodic Signaling (LFPS) burst on the Lane for the duration of at least 5 LFPS cycles and for no more than tLFPSDuration. If the Lane Adapter is in CL1 state, the first LFPS shall be sent within tWarmUpCL1 after receiving the first LFPS cycle. If the Lane Adapter is in CL2 state, the first LFPS shall be sent within tWarmUpCL2 after receiving the first LFPS cycle.
4.2.1.6.5.3#10	TD 4.011 TD 4.013	Upon detecting 2 LFPS cycles, a Lane Adapter in CL1 or CL2 state shall: 2. Return to Electrical Idle for tPreData.
4.2.1.6.5.3#11	TD 4.011 TD 4.013	Upon detecting 2 LFPS cycles, a Lane Adapter in CL1 or CL2 state shall: 3. Start transmitting SLOS1 on the Lane.
4.2.1.6.5.3#12	TD 4.011 TD 4.013	Upon detecting 2 LFPS cycles, a Lane Adapter in CL1 or CL2 state shall: 4. Enable the receiver to start bit and symbol synchronization not earlier than tCLxIdleRx after the last LFPS cycle received. An Adapter shall complete Symbol lock within tRxLock time.
4.2.1.6.5.3#13	TD 4.011 TD 4.013	Upon detecting 2 LFPS cycles, a Lane Adapter in CL1 or CL2 state shall: 5. Upon reception of 3 back-to-back CL_WAKE1.X Ordered Set Symbols, start transmitting CL_WAKE2.X Ordered Set Symbols on the Lane. The Adapter shall ignore any received CL_WAKE2.Y (where Y is any value) Symbols interleaved with CL_WAKE1.X Ordered Set Symbols when it determines the reception of back-to-back CL_WAKE1.X Ordered Set Symbols.

4.2.1.6.5.3#14	TD 4.011 TD 4.013	Upon detecting 2 LFPS cycles, a Lane Adapter in CL1 or CL2 state shall: 6. Upon reception of 7 back-to-back CL_WAKE2.X Ordered Set Symbols or 7 back-to-back SLOS Symbols, transition to Training.LOCK1 sub-state.
4.2.1.6.5.3#15	TD 4.011 TD 4.013	On transition to the TS1 sub-state, the USB4 Port shall enable SSC if SSC is disabled.
<b>4.2.2 USB4 Link Transitions</b>		
4.2.2#1	IOP	A USB4 Link shall operate as either a Single-Lane Link or a Dual-Lane Link.
<b>4.2.2.1 Transition from One Single-Lane Link to Two Single-Lane Links</b>		
4.2.2.1#1	NT	A USB4 Port shall transition from one single-Lane Link to two single-Lane Links when the Lane 1 Adapter is enabled.
<b>4.2.2.2 Transition from Two Single-Lane Link to Dual-Lane Link</b>		
4.2.2.2#1	TD 4.005	A USB4 Port shall transition its Lane Adapters to the Lane Bonding state when all of the following are true: Both Ports are in the Bonding state; The Supported Link Widths field of both Ports is set to x2 support or more; The Target Link Width field of both Ports is set to establish a dual-Lane Link.
4.2.2.2#2	TD 4.005	The Logical Layer shall transition to a Dual-Lane Link when the following conditions are met: Both Adapters have transitioned successfully to CL0 state within tBonding time after sending the first TS1 Ordered Set with <i>Lane Bonding Target</i> set to 001b ; Link Partner has responded with the following value in all TS1 and TS2 Ordered Sets on both Lanes (Lane Bonding Target is set to 001b).
4.2.2.2#3	TD 4.005	If Lane bonding is successful, then a Router shall set the Adapter State field in the Lane Adapter Configuration Capability of the Lane 0 Adapter to CL0.
4.2.2.2#4	TD 4.005	If Lane bonding is successful, then a Router shall set the Negotiated Link Width field in the Lane Adapter Configuration Capability of the Lane 0 Adapter to indicate a USB4 Link width of x2.
4.2.2.2#5	TD 4.005	If Lane bonding is successful, then a Router shall send a Hot Plug Event Packet with the UPG bit set to 1b for the Lane 1 Adapter in the Downstream Facing Port.
4.2.2.2#6	TD 4.035	If one of the Lane Adapters is not in CL0 tBonding time after entry to the Lane Bonding state, the Router shall initiate a Disconnect by driving SBTx to a logical low state for tDisconnectTx.
4.2.2.2#7	TD 4.020	The Adapters of a dual-Lane Link operate in CL0 state in tandem with the following dependencies: Any Ordered Set sent on the Link shall be sent simultaneously on both Lanes within the permitted transmit skew.

4.2.2.2#8	BC	The Adapters of a dual-Lane Link operate in CL0 state in tandem with the following dependencies: When either Adapter of a dual-Lane Link transitions to one of the Training sub-states, the other Adapter in the USB4 Port shall transition to the same Training sub-state.
<b>4.2.2.2.1 Training a Dual-Lane Link</b>		
4.2.2.2.1#1	TD 4.040 TD 4.041	When an Adapter that is part of a dual-Lane Link enters Training state, the other Adapter in the USB4 Port shall enter Training state as well.
4.2.2.2.1#2	TD 4.009	The Logical Layer shall resume dual-Lane Link operation if both Ports meet the transition conditions in Step 6 of the Training state machine in Table 4-20 within tTrainingAbort2 time.
4.2.2.2.1#3	TD 4.009	The Adapter that transitions to the CL0 state first shall send TS2 Ordered Sets until the other Adapter in the USB4 Port exits the training state.
<b>4.2.2.3 Transition from Dual-Lane Link to Two Single-Lane Links</b>		
<b>4.2.2.4 Transition from Two Single-Lane Links to One Single Lane Link</b>		
4.2.2.4#1	TD 4.006	A USB4 Port shall transition from two Single-Lane Links to one Single-Lane Link when one of its Adapters transitions to the Disabled state.
<b>4.2.3 Logical Layer Link States</b>		
<b>4.3 USB4 Link Encoding</b>		
4.3#1	IOP	If RS FEC encoding is off, bytes received from the Transport Layer shall be encoded with either 64b/66b encoding (Gen 2) or 128b/132b encoding (Gen 3)
<b>4.3.1 Lane Distribution</b>		
4.3.1#1	IOP	If a USB4 Link operates as a dual-Lane Link, then distribution of Transport Layer bytes among the Lanes shall alternate as depicted in Figure 4-13.
<b>4.3.2 Symbol Encoding</b>		
<b>4.3.2.1 Symbol Encoding of Transport Layer Bytes</b>		
4.3.2.1#1	NT	A Symbol may contain either Transport Layer bytes or Ordered Set, but shall not contain both

<b>4.3.3 Ordered Sets</b>		
4.3.3#1	IOP	Ordered Set shall have the structure depicted in Table 4-35.
4.3.3#2	IOP	For 64b/66b encoding, an Ordered Set Symbol shall contain a single copy of the Ordered Set payload and 2 Sync Bits.
4.3.3#3	IOP	For 128b/132b encoding, an Ordered Set Symbol shall contain two copies of the Ordered Set (i.e. 64 bits followed by a second copy of the same 64 bits) and 4 Sync Bits.
<b>4.3.4 Bit Swap</b>		
4.3.4#1	IOP	Bit Swap of Transport Layer bytes and of Ordered Sets payload delivered to the scrambler in the order that they are transmitted on the wire.
<b>4.3.4.1 Sync Bits</b>		
4.3.4.1#1	IOP	If RS-FEC is off, all Symbols shall be transmitted Sync Bits first.
4.3.4.1#2	IOP	Sync Bits shall be sent in the order of most significant bit to least significant bit.
4.3.4.1#3	IOP	Transport Layer bytes or Ordered Sets shall be transmitted after the Sync Bits.
<b>4.3.4.2 Data Symbol Payload</b>		
4.3.4.2#1	IOP	The payload within a Data Symbol shall be transmitted from left to right as depicted in Figure 4-18.
4.3.4.2#2	IOP	Within each byte of payload, individual bits shall be transmitted from bit 0 to bit 7.
<b>4.3.4.3 Ordered Set Symbol Payload</b>		
4.3.4.3#1	IOP	When an Ordered Set is longer than 64 bits (i.e. SLOS, CL_WAKE1.X, CL_WAKE2.X), it cannot fit into the payload of one Symbol, and shall be divided into multiple Symbol payloads.
4.3.4.3#2	IOP	The Ordered Set shall be transmitted in increasing Symbols, starting with Symbol 0.
4.3.4.3#3	IOP	Within a Symbol payload, the bytes in an Ordered Set shall be transmitted from left to right as depicted in Figure 4-19.
4.3.4.3#4	IOP	Within each byte, individual bits shall be transmitted from bit 0 to bit 7.
<b>4.3.5 Scrambling</b>		
4.3.5#1	IOP	Scrambling shall be performed according to the rules in Table 4-36.



4.3.5#2	IOP	Scrambling and de-scrambling are performed by passing the encoded bits through an Additive LFSR with a polynomial of $G(X) = X^{23} + X^{21} + X^{16} + X^8 + X^5 + X^2 + 1$ .
4.3.5#3	IOP	The most significant bit of the LFSR is XORed with the data stream on a per-bit basis. The data stream is scrambled in the order that it is sent on wire.
4.3.5#4	IOP	The scrambler shall load a new seed on the following transitions: 1. Transition from LOCK2 sub-state to TS1 sub-state in the Training state; Initial value is 1F EEDDh.
4.3.5#5	IOP	The scrambler shall load a new seed on the following transitions: 2. On exit from CL0s state, before the Adapter initiating exit transmits the first TS2 Ordered Set in the direction exiting electrical idle; Initial value is 1F EEDDh.
4.3.5#6	IOP	The scrambler shall load a new seed on the following transitions: 3. On transition from any state to CL0 when going to a dual-Lane Link; When exiting CL0s state, a new seed shall be loaded only in the direction exiting electrical idle; Initial value on the Lane 0 is 1D BFBCh; Initial value on the Lane 1 is 06 07BBh; The per-Lane seeds are used, starting with the first byte after the de-skew Ordered Set.
4.3.5#8	IOP	Any single-bit errors in the SRC field shall be corrected. If the SCR field contains an uncorrectable error, the Logical Layer reports an OSE error.
<b>4.3.6 RS-FEC</b>		
4.3.6#1	IOP	An Adapter shall support RS-FEC at all speeds.
4.3.6#2	IOP	Each block of 194 bytes shall be generated in the following manner: Transport Layer bytes and Ordered Sets are grouped into 16-byte (128 bit) Symbol payloads. Each Symbol payload may contain either one or more Ordered Set or Transport Layer bytes, but shall not contain both.
4.3.6#3	IOP	Each block of 194 bytes shall be generated in the following manner: When operating at Gen 2 speed, the 16-byte Ordered Set Symbol payload shall contain: For a SLOS Ordered Set, 128 bits of the Ordered Set.
4.3.6#4	IOP	Each block of 194 bytes shall be generated in the following manner: When operating at Gen 2 speed, the 16-byte Ordered Set Symbol payload shall contain: For all other Ordered Sets, two 64-bit Ordered Sets.
4.3.6#5	IOP	When only one Ordered Set needs to be sent, the second Ordered Set shall be a SKIP Ordered Set. See Section 4.4.3 for the structure of a SKIP Ordered Set.
4.3.6#6	IOP	Each block of 194 bytes shall be generated in the following manner: When operating at Gen 3 speed, the 16-byte Ordered Set Symbol payload shall contain: For a SLOS Ordered Set, 128 bits of the Ordered Set.

4.3.6#7	IOP	Each block of 194 bytes shall be generated in the following manner: When operating at Gen 3 speed, the 16-byte Ordered Set Symbol payload shall contain: For all other Ordered Sets, two copies of the Ordered Set (i.e. 64 bits followed by a second copy of the same 64 bits).
4.3.6#8	IOP	Each block of 194 bytes shall be generated in the following manner: The RS-FEC encoder is fed with twelve 16-byte Symbol payloads plus 2 bytes of Sync Bits. Each Symbol is allocated a single Sync Bit, indicating whether it contains Transport Layer bytes (Sync Bit = 0b) or Ordered Set (Sync Bit = 1b).
4.3.6#9	IOP	The 2 bytes of Sync Bits contain 12 active bits (one per 16-byte Symbol) and 4 reserved bits.
4.3.6#10	IOP	Sync Bits shall be delivered to the encoder in order that they will be sent to the wire, from bit 15 to bit 0. The active Sync Bits reside in bits[11:0] of the Word. The Sync Bit corresponding to the oldest 16-byte Symbol resides in bit 0 if the Sync Bits.
4.3.6#11	IOP	The 12 active bits are XORed with 333h before being fed to the RS-FEC encoder. The XORed value is the value seen on the wire.
4.3.6#12	IOP	Each block of 194 bytes shall be generated in the following manner: The RS-FEC encoder generates 4 bytes of redundancy bits (P3 to P0). P3 is the first byte to be sent on the wire and P0 is the last. Within each byte, bits are sent in descending order where bit 7 is sent first and bit 0 is sent last.
4.3.6#13	TD 4.039	The RS-FEC decoder shall correct a received block with up to two 1-byte errors anywhere in the block.
4.3.6#14	NT	An error in a received block that is detectable and uncorrectable shall cause an RDE error.
4.3.6#15	TBD	When operating at Gen 2 speed, the 16-byte Ordered Set Symbol payload shall contain: When a DESKEW Ordered Set is placed first in a 16-byte payload, the second Ordered Set shall be SKIP.
<b>4.3.6.1 RS_FEC Activation and Deactivation</b>		
4.3.6.1#1	IOP	If RS-FEC is enabled during Phase 3 of Lane Initialization, then an Adapter shall activate RS-FEC encoding in the following cases: In Training state, immediately following the last transmitted SLOS2 and before sending the first TS1 Ordered Set.
4.3.6.1#2	IOP	If RS-FEC is enabled during Phase 3 of Lane Initialization, then an Adapter shall activate RS-FEC encoding in the following cases: During exit from CL0s state, immediately before sending the first TS2 Ordered Set.
4.3.6.1#3	IOP	A START_RS_FEC bit sequence shall be sent prior to activating RS-FEC encoding on the Lane.
4.3.6.1#4	IOP	The bit sequence shall not be scrambled and shall not advance the scrambler LFSR.

4.3.6.1#5	IOP	The START_RS_FEC bit sequence shall be sent with bit[31] first on the wire.
4.3.6.1#6	IOP	During exit from CL0s state, the START_RS_FEC bit sequence shall only be sent in the direction exiting electrical idle.
4.3.6.1#7	IOP	The bit following the START_RS_FEC bit sequence shall be the first bit to be RS-FEC encoded.
4.3.6.1#8	IOP	If RS-FEC encoding is activated, a USB4 Port shall deactivate RS-FEC encoding on a Lane in the following cases: When to Training state, after transmitting n SLOS1 Symbols in LOCK1 sub-state with RS-FEC on, where $32 \leq n \leq 64$ in Gen 2 and $16 \leq n \leq 32$ in Gen 3.
4.3.6.1#9	IOP	If RS-FEC encoding is activated, a USB4 Port shall deactivate RS-FEC encoding on a Lane in the following cases: Entry to Disabled state.
4.3.6.1#10	IOP	If RS-FEC encoding is activated, a USB4 Port shall deactivate RS-FEC encoding on a Lane in the following cases: Entry to CLd state.
4.3.6.1#11	IOP	If RS-FEC encoding is activated, a USB4 Port shall deactivate RS-FEC encoding on a Lane in the following cases: Entry to CL0s state, in the direction entering low power state.
4.3.6.1#12	IOP	If RS-FEC encoding is activated, a USB4 Port shall deactivate RS-FEC encoding on a Lane in the following cases: Entry to CL2 or CL1 states.
4.3.6.1#13	IOP	If RS-FEC encoding is activated, a USB4 Port shall deactivate RS-FEC encoding on a Lane in the following cases: Entry to Training.LOCK2 sub-state.
<b>4.3.6.2 Pre-Coding</b>		
4.3.6.2#1	IOP	If pre-coding is on, then before each bit is sent on the wire, it shall be XOR'ed with the bit sent before it, using the value of the bit after it was coded.
4.3.6.2#2	IOP	Pre-coding shall be turned on with the first bit that is RS_FEC encoded.
4.3.6.2#3	IOP	Pre-coding shall be turned off with the first bit that is not RS_FEC encoded.
<b>4.4 USB4 Link Operation</b>		
<b>4.4.1 Start of Data</b>		
4.4.1#1	BC	When an Adapter transitions to CL0 state, the first transmitted bytes after the last TS2 Ordered Set shall be either a Transport Layer header, an Idle Packet or any Ordered Set other than SLOS, TS1 or TS2.
4.4.1#2	BC	For a dual-Lane Link, the first transmitted bytes after the last TS2 Ordered Set shall be a de-skew Ordered Set followed by either a Transport Layer header, an Idle Packet or any Ordered Set other than SLOS, TS1 or TS2.

4.4.2 Error Cases and Recovery		
4.4.2#1	TD 4.040	A Router shall support the Ordered Set Errors (OSE) error case.
4.4.2#2	TD 4.040	When a Router supports an error case, it shall do so as described in this section.
4.4.2#3	TD 4.040	A Router shall support the same error cases on all Lane Adapters.
4.4.2#4	TD 4.040	When an Adapter supports an error case, it shall support that error case in all Adapter states unless specified otherwise.
4.4.2#5	NT	If an Adapter reports Alignment Lock Errors, when an Adapter receives N number of Symbols in a row with illegal Sync Bits values, where N is a number between 1 and 8 (inclusive) that is chosen by the implementation, it shall go to Training.LOCK1 sub-state.
4.4.2#6	NT	If an Adapter reports Alignment Lock Errors, when an Adapter receives a Symbol with illegal Sync bit values, it shall set the ALE bit in the Logical Layer Errors field to 1b.
4.4.2#7	NT	If an Adapter reports Alignment Lock Errors, when an Adapter receives a Symbol with illegal Sync bit values, if the ALE bit in the Logical Layer Errors Enable field is 1b, the Router shall send a Notification Packet with Event Code = ERR_LINK to the Connection Manager.
4.4.2#8	NT	If an Adapter reports Alignment Lock Errors, when an Adapter receives a Symbol with illegal Sync bit values, if the ALE bit in the Logical Layer Errors Enable field is 0b, the Router shall not send a Notification Packet.
4.4.2#9	TD 4.040	If an Adapter reports Ordered Set Errors, when it receives 2 back-to-back Symbols that contain an Ordered Set that is not defined in this specification and/or have an uncorrectable error in the SRC field, it shall go to Training.LOCK1 sub-state.
4.4.2#10	TD 4.040 TD 4.041	If an Adapter reports Ordered Set Errors, when it receives 2 back-to-back Symbols that are not part of an Ordered Set defined in this specification and/or have an uncorrectable error in the SRC field, it shall set the OSE bit in the Logical Layer Errors field to 1b.
4.4.2#11	TD 4.040 TD 4.041	If an Adapter reports Ordered Set Errors, when it receives 2 back-to-back Symbols that are not part of an Ordered Set defined in this specification and/or have an uncorrectable error in the SRC field, if the OSE bit in the Logical Layer Errors Enable field is 1b, the Router shall send a Notification Packet with Event Code = ERR_LINK to the Connection Manager.
4.4.2#12	TD 4.040 TD 4.041	If an Adapter reports Ordered Set Errors, when it receives 2 back-to-back Symbols that are not part of an Ordered Set defined in this specification and/or have an uncorrectable error in the SRC field, if the OSE bit in the Logical Layer Errors Enable field is 0b, the Router shall not send a Notification Packet.

4.4.2#13	NT	If an Adapter reports Timeout Errors, when an Adapter entered Training state from either CL0, CL1, or CL2 state and did not transition to CL0 state within tTrainingError after sending the first SLOS1.
4.4.2#14	NT	If an Adapter reports Timeout Errors, when an Adapter does not transition from Training state to CL0 state within tTrainingError after achieving Symbol alignment, it shall set the TE bit in the Logical Layer Errors field to 1b.
4.4.2#15	TD 4.042	If an Adapter reports Timeout Errors, when an Adapter does not transition from Training state to CL0 state within tTrainingError after achieving Symbol alignment, if the TE bit in the Logical Layer Errors Enable field is 1b, the Router shall send a Notification Packet with Event Code = ERR_LINK to the Connection Manager.
4.4.2#16	TD 4.042	If an Adapter reports Timeout Errors, when an Adapter does not transition from Training state to CL0 state within tTrainingError after achieving Symbol alignment, if the TE bit in the Logical Layer Errors Enable field is 0b, the Router shall not send a Notification Packet.
4.4.2#17	NT	If an Adapter reports Elastic Buffer Errors, when the elastic buffer is full, it shall: go to Training.LOCK1 sub-state.
4.4.2#18	NT	If an Adapter reports Elastic Buffer Errors, when the elastic buffer is full, it shall set the EBE bit in the Logical Layer Errors field to 1b.
4.4.2#19	NT	If an Adapter reports Elastic Buffer Errors, when the elastic buffer is full, if the EBE bit in the Logical Layer Errors Enable field is 1b, the Router shall send a Notification Packet with Event Code = ERR_LINK to the Connection Manager (see Section 6.5).
4.4.2#20	NT	If an Adapter reports Elastic Buffer Errors, when the elastic buffer is full, if the EBE bit in the Logical Layer Errors Enable field is 0b, the Router shall not send a Notification Packet.
4.4.2#21	NT	If an Adapter reports De-skew Buffer Errors, when skew is too large resulting in overflow in the de-skew buffer, it shall set the DBE bit in the Logical Layer Errors field to 1b.
4.4.2#22	NT	If an Adapter reports De-skew Buffer Errors, when skew is too large resulting in overflow in the de-skew buffer, if the DBE bit in the Logical Layer Errors Enable field is 1b, the Router shall send a Notification Packet with Event Code = ERR_LINK to the Connection Manager.
4.4.2#23	NT	If an Adapter reports De-skew Buffer Errors, when skew is too large resulting in overflow in the de-skew buffer, if the DBE bit in the Logical Layer Errors Enable field is 0b, the Router shall not send a Notification Packet.
4.4.2#24	NT	If an Adapter reports RS-FEC decoder errors, when the RS-FEC decoder identifies an uncorrectable error, it shall turn off RS-FEC in both directions of the Link.

4.4.2#25	NT	If an Adapter reports RS-FEC decoder errors, when the RS-FEC decoder identifies an uncorrectable error, it shall set the RDE bit in the Logical Layer Errors field to 1b.
4.4.2#26	NT	If an Adapter reports RS-FEC decoder errors, when the RS-FEC decoder identifies an uncorrectable error, if the RDE bit in the Logical Layer Errors Enable field is 1b, the Router shall send a Notification Packet with Event Code = ERR_LINK to the Connection Manager.
4.4.2#27	NT	If an Adapter reports RS-FEC decoder errors, when the RS-FEC decoder identifies an uncorrectable error, if the RDE bit in the Logical Layer Errors Enable field is 0b, the Router shall not send a Notification Packet.
4.4.2#28	NT	If an Adapter reports RX Sync Timeout, if, while in LOCK1 sub-state of the Training state, the receiver cannot lock on Sync Bits for an implementation-specific period of time, it shall remain in LOCK1 sub-state.
4.4.2#29	NT	If an Adapter reports RX Sync Timeout, if, while in LOCK1 sub-state of the Training state, the receiver cannot lock on Sync Bits for an implementation-specific period of time, it shall set the RST bit in the Logical Layer Errors field to 1b.
4.4.2#30	NT	If an Adapter reports RX Sync Timeout, if, while in LOCK1 sub-state of the Training state, the receiver cannot lock on Sync Bits for an implementation-specific period of time, if the RST bit in the Logical Layer Errors Enable field is 1b, the Router shall send a Notification Packet with Event Code = ERR_LINK to the Connection Manager.
4.4.2#31	NT	If an Adapter reports RX Sync Timeout, if, while in LOCK1 sub-state of the Training state, the receiver cannot lock on Sync Bits for an implementation-specific period of time, if the RST bit in the Logical Layer Errors Enable field is 0b, the Router shall not send a Notification Packet.
<b>4.4.3 Clock Compensation and SKIP</b>		
4.4.3#1	IOP	A receiver shall drop any received SKIP Ordered Sets and shall be capable of operating in the absence of any SKIP Ordered sets.
4.4.3#2	IOP	A Transmitter shall not send SKIP Ordered Sets while the Adapter is in the Training.LOCK1 or Training.LOCK2 sub-states.
4.4.3#3	IOP	A SKIP Ordered Set shall have the structure defined in Table 4-39.
4.4.3#4	IOP	SCR – Shall be set to 11 0000 1101b to indicate that the Ordered Set contents are not scrambled.
<b>4.4.4 Dual-Lane Skew</b>		
4.4.4#1	TD 4.043	A Router shall operate with skew defined in Section 3.5.1 between the receiving Lanes of a Link when measured at the USB Type-C connector.
4.4.4#2	NT	A transmitter shall not introduce skew more than defined in Section 3.4.1.

4.4.4#3	TD 4.009	A single de-skew Ordered Set shall be sent on each Lane after both Adapters transition (from any state) to CL0 state, and the USB4 Port in Dual-Lane Link mode.
4.4.4#4	TD 4.009	When exiting CL0s state, a de-skew Ordered Set shall only be sent in the direction exiting electrical idle.
4.4.4#5	TBD	When a Port operates at Gen 3 speed, the De-Skew Ordered Set shall be transmitted twice. Otherwise it shall be transmitted once.
4.4.4#6	TD 4.009	A de-skew Ordered Set shall be sent simultaneously on both Lanes within the permitted transmit skew
4.4.4#7	TD 4.009	A de-skew Ordered Set shall be sent on both Lanes in the same locations within the Symbol.
4.4.4#8	TD 4.009	The de-skew Ordered Set shall be the first bytes sent after the TS2 Ordered Sets.
4.4.4#9	TD 4.009	TS2 Ordered Sets shall be transmitted on a Lane in CL0 state until the de-skew Ordered Set is sent.
4.4.4#10	NT	SCR in the De-Skew Ordered Set payload shall be set to 00 1111 0010b to indicate that the Ordered Set contents are scrambled.
<b>4.4.5 Disconnect</b>		
<b>4.4.5.1 Upstream Facing Port Disconnect</b>		
<b>4.4.5.1.1 SBRX Goes Low</b>		
4.4.5.1.1#1	TD 4.017	The Router with the disconnected Port shall: Drive SBTX to a logical low state on all USB4 Ports for tDisconnectTx.
4.4.5.1.1#2	TD 4.017	The Router with the disconnected Port shall: Transition to the Uninitialized Unplugged state.
4.4.5.1.1#3	CH6	The following events initiate a disconnect as defined in this section: Router Hot Unplug.
4.4.5.1.1#4	CH6	The following events initiate a disconnect as defined in this section: Downstream Facing Port Reset where the Link Partner is an Upstream Facing Port.
4.4.5.1.1#5	NT	The following events initiate a disconnect as defined in this section: The Domain enters Sleep state, the USB4 Port is Configured bit in a USB4 Port is set to 0b, and the Link Partner is an Upstream Facing Port.
4.4.5.1.1#6	TBD	The following events initiate a disconnect as defined in this section: The Link Partner failed to train the Link before the defined timeout.

4.4.5.1.1#7	TBD	The following events initiate a disconnect as defined in this section: The Lane bonding did not complete before the defined timeout.
<b>4.4.5.1.2 LT_Fall Transaction is Received</b>		
<b>4.4.5.1.3 LT_LRoff Transaction is Received on an Upstream Facing Port</b>		
4.4.5.1.3#1	NT	When an Upstream Facing Port receives an LT_LRoff transaction and the <i>Enter Sleep</i> bit in the Router Configuration Space is set to 0b, the Port is disconnected. The disconnected Port shall send an LT_LRoff Transaction.
4.4.5.1.3#2	NT	The Router with the disconnected Port shall: Drive SBTX to a logical low state on all USB4 Ports for tDisconnectTx.
4.4.5.1.3#3	NT	The Router with the disconnected Port shall: Transition to the Uninitialized Unplugged state.
4.4.5.1.3#4	NT	The following events shall initiate a disconnect as defined in this section: The Domain enters Sleep state, in the Downstream Facing Port of the Link Partner the USB4 Port is Configured bit is 0b and the Enable Wake on Connect bit of the USB4 Port is 1b.
<b>4.4.5.2 Downstream Port Disconnect</b>		
<b>4.4.5.2.1 SBRX Goes Low</b>		
4.4.5.2.1#1	TD 4.018	When a Downstream Facing Port detects SBRX at logical low state for tDisconnectRx and its <i>Lane Disable</i> bit in the Lane 0 Adapter Configuration Capability is set to 0b, the Port is disconnected and shall: Send an LT_LRoff Transaction.
4.4.5.2.1#2	TD 4.018	When a Downstream Facing Port detects SBRX at logical low state for tDisconnectRx and its <i>Lane Disable</i> bit in the Lane 0 Adapter Configuration Capability is set to 0b, the Port is disconnected and shall: Discard any Transport Layer Packets received from the Ingress Port(s) on the Router.
4.4.5.2.1#3	TD 4.018	When a Downstream Facing Port detects SBRX at logical low state for tDisconnectRx and its <i>Lane Disable</i> bit in the Lane 0 Adapter Configuration Capability is set to 0b, the Port is disconnected and shall: Transition its Adapters to the CLd state
4.4.5.2.1#4	NT	The Router with the disconnected Port shall continue to send flow control Packets on the Ingress Port(s) for Transport Layer Packets that the disconnected Port discarded.
4.4.5.2.1#5	NT	Flow control credit counts shall be updated as if the discarded packets were dequeued and forwarded to the Egress Adapter.
4.4.5.2.1#6	TD 4.018	The Router shall do the following for each enabled Lane Adapter in the disconnected Port: Send the Connection Manager a Hot Plug Event Packet with the <i>UPG</i> bit set to 1b.



4.4.5.2.1#7	TD 4.006 TD 4.018	The Router shall do the following for each enabled Lane Adapter in the disconnected Port: Load the following fields in the Adapter Configuration Space with their default values: Basic Configuration Registers: Link Credits Allocated; TMU Adapter Configuration Capability: Inter-Domain Time Initiator, EnableUniDirectionalMode; Lane Adapter Configuration Capability: Target Link Width, CL0s Enable, CL1 Enable, CL2 Enable, Lane Bonding.
4.4.5.2.1#8	NT	The Router shall do the following for each enabled Lane Adapter in the disconnected Port: Load the TxFFE register in the SB Register Space with its default values.
<b>4.4.5.2.2 LT_LRoff Transaction is Received</b>		
4.4.5.2.2#1	NT	When a Downstream Facing Port receives an LT_LRoff Transaction, the Lane Disabled bit in the Lane 0 Adapter Configuration Capability is set to 0b, and the <i>Enter Sleep</i> bit in the Router Configuration Space is set to 0b, the Port is disconnected and shall: Send an LT_LRoff Transaction.
4.4.5.2.2#2	NT	When a Downstream Facing Port receives an LT_LRoff Transaction and the <i>Enter Sleep</i> bit in the Router Configuration Space is set to 0b, the Port is disconnected and shall: Discard any Transport Layer Packets received from the Ingress Port(s) on the Router.
4.4.5.2.2#3	NT	When a Downstream Facing Port receives an LT_LRoff Transaction and the <i>Enter Sleep</i> bit in the Router Configuration Space is set to 0b, the Port is disconnected and shall: Transition its Adapters to the CLd state.
4.4.5.2.2#4	NT	The Router with the disconnected Port shall continue to send flow control Packets on the Ingress Port(s) for Transport Layer Packets that the disconnected Port discarded.
4.4.5.2.2#5	NT	Flow control credit counts shall be updated as if the discarded packets were dequeued and forwarded to the Egress Adapter.
4.4.5.2.2#6	NT	The Router shall do the following for each enabled Lane Adapter in the disconnected Port: Send the Connection Manager a Hot Plug Event Packet with the UPG bit set to 1b.
4.4.5.2.2#7	NT	The Router shall do the following for each enabled Lane Adapter in the disconnected Port: Load the following fields in Adapter Configuration Space with their default values: Basic Configuration Registers: Link Credits Allocated; TMU Adapter Configuration Capability: Inter-Domain Time Initiator, EnableUniDirectionalMode; Lane Adapter Configuration Capability: Target Link Width CL0s Enable CL1 Enable CL2 Enable Lane Bonding.
4.4.5.2.2#8	NT	The Router shall do the following for each enabled Lane Adapter in the disconnected Port: Load the TxFFE register in SB Register Space with its default values.
4.4.5.2.2#9	NT	The Router shall do the following for each enabled Lane Adapter in the disconnected Port: Start Lane Initialization from Phase 2.

4.4.6 Lane Adapter Disable and Enable		
4.4.6.1 Disabled Adapter is the Upstream Adapter		
4.4.6#1	NT	After the <i>Lane Disable</i> bit in its Upstream Adapter is set to 1b, a Router shall: 1. Send an LT_Fall Transaction to the Link Partner of the Upstream Facing Port to signal transition to the Disabled state.
4.4.6#2	NT	After the <i>Lane Disable</i> bit in its Upstream Adapter is set to 1b, a Router shall: 2. Drive SBTx to a logical low state on all USB4 Ports for tDisconnectTx.
4.4.6#3	NT	After the <i>Lane Disable</i> bit in its Upstream Adapter is set to 1b, a Router shall: 3. Transition to the Uninitialized Unplugged state.
4.4.6#4	NT	After the <i>Lane Disable</i> bit in its Upstream Adapter is set to 1b, a Router shall: 4. Start Lane Initialization from Phase 1.
4.4.6#5	NT	After the <i>Lane Disable</i> bit in its Upstream Adapter is set to 1b, a Router shall: 5. After detecting a Router on the Upstream Facing Port, transition to the Uninitialized Plugged state.
4.4.6.2 Disabled Adapter is not the Upstream Adapter		
4.4.6.2.1 Disable Flow		
4.4.6.2.1#1	NT	After the <i>Lane Disable</i> bit in the Adapter Configuration Space of the Lane Adapter is set to 1b, the Router shall: 1. Send an LT_Fall Transaction to the Link Partner of the Upstream Facing Port to signal transition to the Disabled state.
4.4.6.2.1#2	NT	After the <i>Lane Disable</i> bit in the Adapter Configuration Space of the Lane Adapter is set to 1b, the Router shall: 2. Send a Hot Plug Event Packet for the disabled Adapter with the UPG bit set to 1b to the Connection Manager.
4.4.6.2.1#3	TD 4.006	After the <i>Lane Disable</i> bit in the Adapter Configuration Space of the Lane Adapter is set to 1b, the Router shall: 3. Transition the Adapter to the Disabled State.
4.4.6.2.1#4	NT	After the <i>Lane Disable</i> bit in the Adapter Configuration Space of the Lane Adapter is set to 1b, the Router shall: 4. If the Router detects that SBRx of the disabled Adapter transitions to a low logical state for more than tDisconnectRx, the Router shall perform the disconnect flow defined in Section 4.4.5.2.1.
4.4.6.2.1.1 Link Partner is not the Upstream Adapter		
4.4.6.2.1.1#1	TD 4.007	If the Link Partner of the disabled Adapter is not the Upstream Adapter, it shall do the following upon receiving the LT_Fall Transaction: 1. Send a Hot Plug Event Packet with the UPG bit set to 1b to the Connection Manager.

4.4.6.2.1.1#2	TD 4.006 TD 4.007	If the Link Partner of the disabled Adapter is not the Upstream Adapter, it shall do the following upon receiving the LT_Fall Transaction: 2. Load the following fields in the Adapter Configuration Space of the Adapter with their default values: Basic Configuration Registers: Link Credits Allocated; TMU Adapter Configuration Capability: Inter-Domain Time Initiator; USB4 Port Configuration Capability: Target Link Width CL0s Enable CL1 Enable CL2 Enable Lane Bonding.
4.4.6.2.1.1#3	NT	If the Link Partner of the disabled Adapter is not the Upstream Adapter, it shall do the following upon receiving the LT_Fall Transaction: 3. Transition to the CLd state.
<b>4.4.6.2.1.2 Link Partner is the Upstream Adapter</b>		
4.4.6.2.1.2#1	TD 4.007	If the Link Partner of the disabled Adapter is the Upstream Adapter, it shall do the following upon receiving the LT_Fall Transaction: 1. Drive SBTx to a logical low state on all USB4 Ports for tDisconnectTx.
4.4.6.2.1.2#2	TD 4.007	If the Link Partner of the disabled Adapter is the Upstream Adapter, it shall do the following upon receiving the LT_Fall Transaction: 2. Transition to the Uninitialized Unplugged state.
4.4.6.2.1.2#3	NT	If the Link Partner of the disabled Adapter is the Upstream Adapter, it shall do the following upon receiving the LT_Fall Transaction: 3. Transition to the Uninitialized Plugged state as a result of detecting SBRX driven high.
4.4.6.2.1.2#4	TD 4.007	If the Link Partner of the disabled Adapter is the Upstream Adapter, it shall do the following upon receiving the LT_Fall Transaction: 4. Start lane Initialization from Phase 1.
<b>4.4.6.2.2 Enable Flow</b>		
<b>4.4.7 Time Sync Notification Ordered Set (TSNOS)</b>		
4.4.7#1	NT	When a Router receives a Time Sync Notification Ordered Set (TSNOS) it shall generate a time stamp.
4.4.7#2	NT	The Time Sync Notification Ordered Set shall have the structure in Table 4-41.
4.4.7#3	NT	SCR in the Time Sync Notification Ordered Set payload shall be set to 11 0000 1101b to indicate that the Ordered Set contents are not scrambled.
<b>4.5 Sleep and Wake</b>		
<b>4.5.1 Entry to Sleep</b>		
4.5.1#1	NT	Deprecated.
4.5.1#2	CH11	Deprecated.

4.5.1#3	NT	(Host Router) A Router shall enter sleep state when the <i>Enter Sleep</i> bit is set to 1b and one of the following sleep events occur: The Router receives an implementation-specific signal indicating entry to Sleep state.
4.5.1#4	CH11	(Device Router) A Router shall enter sleep state when the Enter Sleep bit is set to 1b and one of the following sleep events occur: The Router tunnels PCIe traffic and receives a PERST Active Tunneled Packet on the Upstream Facing Port.
4.5.1#5	NT	(Device Router) A Router shall enter sleep state when the Enter Sleep bit is set to 1b and one of the following sleep events occur: The Router receives an LT_LRoff Transaction on the Sideband Channel of an Upstream Facing Port.
4.5.1#6	NT	A Router shall not enter sleep state unless the Enter Sleep bit is set to 1b before a sleep event occurs.
4.5.1#7	NT	After the Enter Sleep bit is set to 1b, the Router shall complete any pending transactions on the Sideband Channel.
4.5.1#8	NT	When the Router is ready for the sleep event it shall set the <i>Sleep Ready</i> bit to 1b.
4.5.1#9	NT	After a sleep event occurs, the Router shall do the following for each USB4 Port: If the <i>USB4 Port is inter-Domain</i> bit is 0b and the <i>USB4 Port is Configured</i> bit is 0b, perform a disconnect by driving its SBTX line low for tDisconnectTx. If the <i>Enable Wake on Connect</i> bit of the USB4 Port is 1b, the USB4 Port shall drive its SBTX line high after tDisconnectTx.
4.5.1#10	NT	After a sleep event occurs, the Router shall do the following for each USB4 Port: If the USB4 Port is inter-Domain bit is 1b and the Enable Wake on inter-Domain bit is set to 0b, perform a disconnect by driving its SBTX line low for tDisconnectTx.
4.5.1#11	CH11	After a sleep event occurs, the Router shall do the following for each USB4 Port: Else: If the Router supports PCIe Tunneling, send at least 3 PERST Active Tunneled Packets on all Downstream PCIe Adapters that have the <i>Path Enable</i> bit set to 1b.
4.5.1#12	NT	After a sleep event occurs, the Router shall do the following for each USB4 Port: Else: Send an LT_LRoff Transaction on the Sideband Channel within tLRoffResponse from detecting the sleep event.
4.5.1#13	NT	After a sleep event occurs, the Router shall do the following for each USB4 Port: Else: If the <i>USB4 Port is Inter-Domain</i> bit is 0b and the <i>USB4 Port is Configured</i> bit is 1b, wait for an LT_LRoff Transaction on the Sideband Channel, unless an LT_LRoff Transaction was already received from the time the <i>Enter Sleep</i> bit was set to 1b.
4.5.1#14	NT	After a sleep event occurs, the Router shall do the following for each USB4 Port: Else: Transition the Adapters to CLd state.

4.5.2 Behavior in Sleep State		
4.5.2#1	NT	On entry to sleep state, a Router shall restore all Configuration Spaces to their default values.
4.5.2#2	NT	If the Enter Sleep bit is set to 1b, a Router shall retain a copy of the state information listed in Table 4-42 separate from Configuration Space.
4.5.2#3	NT	If a USB4 Port has the USB4 Port is inter-Domain state set to 1b, then the USB4 Port shall ignore any Transactions received on the Sideband Channel while in Sleep state.
4.5.3 Wake Events		
4.5.3#1	NT	A Router shall issue a Wake on Connect if the Enable Wake on Connect bit of a USB4 Port is set to 1b, the USB4 Port is Configured bit is 0b, the USB4 Port is Inter-Domain bit is set to 0b, and it detects either of the following after the Enter Sleep bit is set to 1b and it detects either of the following: A connection on the USB Type-C connector attached to the USB4 Port.
4.5.3#2	NT	A Router shall issue a Wake on Connect if the Enable Wake on Connect bit of a USB4 Port is set to 1b, the USB4 Port is Inter-Domain bit is set to 0b, and it detects either of the following: SBRX is at logic high on the USB4 Port for tConnectRx.
4.5.3#3	IOP	A Router shall issue a Wake on Disconnect event if the Enable Wake on Disconnect bit of a USB4 Port is set to 1b, the USB4 Port is Inter-Domain bit is set to 0b, the USB4 Port is Configured bit is set to 1b, and the Router detects either of the following after the Enter Sleep bit is set to 1b: A disconnect on the USB Type-C connector attached to the USB4 Port.
4.5.3#4	IOP	A Router shall issue a Wake on Disconnect event if the <i>Enable Wake on Disconnect</i> bit of a USB4 Port is set to 1b, the <i>USB4 Port is Inter-Domain</i> bit is set to 0b, the <i>USB4 Port is Configured</i> bit is set to 1b, and the Router detects either of the following after the <i>Enter Sleep</i> bit is set to 1b: SBRX is at logic low on the USB4 Port for tDisconnectRx.
4.5.3#5	IOP	A Router shall issue a Wake on Inter-Domain event if the Enable Wake on Inter-Domain bit is set to 1b, the USB4 Port is Inter-Domain bit is set to 1b, and the Router detects either of the following after the Enter Sleep bit is set to 1b: A disconnect on the USB Type-C connector attached to the USB4 Port.
4.5.3#6	IOP	A Router shall issue a Wake on Inter-Domain event if the Enable Wake on Inter-Domain bit is set to 1b, the USB4 Port is Inter-Domain bit is set to 1b, and the Router detects either of the following after the Enter Sleep bit is set to 1b: SBRX is at logic low on the USB4 Port for tDisconnectRx.
4.5.3#7	CH11	A Router shall issue a Wake on PCIe event if the Enable Wake on PCIe bit is set to 1b, and it detects a PCIe Wake event from any connected PCIe Endpoint or Switch after a Sleep Event occurs.

4.5.3#8	CH11	A Router shall issue a Wake on USB3 event if the Enable Wake on USB3 bit is set to 1b, and it detects a USB Wake event from any connected USB device after a Sleep Event occurs.
4.5.3#9	IOP	A Router shall issue a Wake on USB4 event if the USB4 Port is inter-Domain bit is set to 0b, the USB4 Port is Configured bit is set to 1b, and the Router detects at least one transition of SBRX to logical low for tWake time after a Sleep Event occurs.
4.5.3#10	TBD	A Router shall issue a Wake on DP event if the Enable Wake on DP bit is set to 1b, and it detects an HPD change or reception of an HPD IRQ after a Sleep Event occurs.
4.5.3#11	TBD	A Host Router shall issue a Wake by Host System when it detects an implementation-specific wake indication from the host system.
<b>4.5.4 Exit from Sleep</b>		
<b>4.5.4.1 Upstream Facing Port Disconnect</b>		
4.5.4.1#1	NT	When a Router detects a disconnect on the UFP, it shall exit sleep state
<b>4.5.4.2 Wake on USB4 Event</b>		
4.5.4.2#1	IOP	A Router shall assert SBRX to logical low for tWake time to indicate a Wake on USB4 event.
4.5.4.2#2	NT	After detecting a wake event, a Router shall: 1. issue a Wake on USB4 event on all connected USB4 Ports by asserting SBTX to logical low for tWake time.
4.5.4.2#3	NT	After detecting a wake event, a Router shall: 2. begin Lane Initialization on all connected USB4 Ports.
4.5.4.2#4	NT	The transmitting USB4 Port shall retry the Transactions as defined in Section 4.1.1.2.5.
4.5.4.2#5	NT	After detecting a wake event, the Router shall: 3. for every Adapter that reaches CL0 state, send a Hot Plug Event Packet to the Connection Manager with the UPG bit set to 0b.
<b>4.6 Timing Parameters</b>		

## Chapter 8

Assertion #	Test Name	Assertion Description
<b>8 Configuration Spaces</b>		
<b>8.2 Configuration Spaces</b>		
<b>8.2.2 Adapter Configuration Space</b>		
<b>8.2.2.3 Lane Adapter Configuration Capability</b>		
8.2.2.3#21	TD 4.005	The Negotiated Link Width field shall indicate the negotiated Link width (xN – corresponding to N Lanes).
<b>8.2.2.4 USB4 Port Capability</b>		
8.2.2.4#21	NT	An Adapter shall set the Router Detected bit to 1b when the USB4 Port detects a connected Router.
8.2.2.4#22	NT	An Adapter shall set the Router Detected bit to 0b upon a disconnect.
8.2.2.4#23	NT	An Adapter shall set the Wake on Connect Status bit to 1b after a wake event is generated by the USB4 Port as a result of a connect to the USB4 Port.
8.2.2.4#24	NT	The Wake on Connect Status bit shall not be set to 1b unless the Enable Wake on Connect bit is 1b.
8.2.2.4#25	NT	The Wake on Connect Status bit shall be set to 0b on entry to sleep.
8.2.2.4#26	NT	An Adapter shall set the Wake on Disconnect Status bit to 1b after a wake event is generated by the USB4 Port as a result of a disconnect from the USB4 Port.
8.2.2.4#27	NT	The Wake on Disconnect Status bit shall not be set to 1b unless the Enable Wake on Disconnect bit is 1b.
8.2.2.4#28	NT	The Wake on Disconnect Status bit shall be set to 0b on entry to sleep.
8.2.2.4#29	NT	An Adapter shall set the <i>Wake on USB4 Wake Status</i> bit to 1b after a wake event is generated by the USB4 Port as a result of a USB4 Wake.
8.2.2.4#30	NT	The <i>Wake on USB4 Wake Status</i> bit shall not be set to 1b unless the <i>Enable Wake on USB4 Wake</i> bit is 1b.
8.2.2.4#31	NT	The <i>Wake on USB4 Wake Status</i> bit shall be set to 0b on entry to sleep.
8.2.2.4#32	NT	An Adapter shall set the Wake on Inter-Domain Status bit to 1b after a wake event is generated by the USB4 Port as a result of an inter-Domain Wake.

8.2.2.4#33	NT	The Wake on Inter-Domain Status bit shall not be set to 1b unless the Enable Wake on inter-Domain bit is 1b.
8.2.2.4#34	NT	The Wake on Inter-Domain Status bit shall be set to 0b on entry to sleep.



## Chapter 13

The following Table presents the USB4 Specification Chapter 13 asserts.

Assertion #	Test Name	Assertion Description
<b>13 Interoperability with Thunderbolt™ 3 (TBT3) Systems</b>		
<b>13.2 Logical Layer</b>		
<b>13.2.1 Sideband Channel</b>		
<b>13.2.1.1 Bidirectional Re-timer</b>		
13.2.1.1#1	IOP	A Router shall implement a bidirectional Sideband Channel when attached directly to a bidirectional Cable Re-timer.
13.2.1.1#2	IOP	A Router shall implement a unidirectional Sideband Channel when not attached directly to a bidirectional Cable Re-timer.
13.2.1.1#3	IOP	A Router that is connected directly to a bidirectional Re-timer shall support concurrent reception of Transactions on SBTX and on SBRX.
13.2.1.1#4	NT	A Router shall drive its SBTX for up to 2 bit times after the last Stop bit of an AT Command.
<b>13.2.1.2 Transactions</b>		
<b>13.2.1.2.1 LT Transactions</b>		
13.2.1.2.1#1	IOP	A Router shall support the additional LT Transaction types defined in Table 13-2.
<b>13.2.1.2.2 AT Transactions</b>		
13.2.1.2.2#1	BC	The structure of the STX Symbol within an AT Transaction shall be as defined in Table 13-3.
13.2.1.2.2#2	NT	Bit 4 in the STX symbol (Responder) shall be set to 1b by a Re-timer in an AT Response when operating in an active cable with bidirectional Re-timers.
13.2.1.2.2#3	BC	Bit 4 in the STX symbol (Responder) shall be set to 0b in all other cases.
13.2.1.2.2#4	NT	Bit 2 in the STX symbol (Recipient): For an AT Command: shall be 0b if a Cable Re-timer is the intended final recipient or 1b if a Router is the intended final recipient
13.2.1.2.2#5	BC	Bit 2 in the STX symbol (Recipient): For an AT Response: shall be set to 1b

13.2.1.2.2#6	NT	A Router shall not send an AT Command that targets Register 13 of a Re-timer or Router SB Register Space unless the Re-timer or Router is directly attached to it.
<b>13.2.1.2.2.1 Bounce Mechanism</b>		
13.2.1.2.2.1#1	TD 13.1.001	A Router shall support the Bounce Mechanism.
13.2.1.2.2.1#2	TD 13.1.001	A Router shall set the Bounce bit to 1b and the ReturnBounce bit to 1b to target a Cable Re-timer that is adjacent to the Router's Link Partner.
13.2.1.2.2.1#3	TD 13.1.001	A Router that receives an AT Transaction with the Bounce bit set to 1b and the ReturnBounce bit to 1b shall set the Bounce bit to 0b, then forward the AT Transaction towards its adjacent Cable Re-timer.
13.2.1.2.2.1#4	TD 13.1.001	A Router that receives an AT Response with the Bounce bit set to 1b and the ReturnBounce bit to 0b shall set the Bounce bit to 0b, then forward the AT Response to its Link Partner.
<b>13.2.1.2.3 RT Transactions</b>		
13.2.1.2.3#1	BC	Byte 2 in a Broadcast RT Transaction shall have the format in Table 4-7 with the changes in Table 13-4.
<b>13.2.1.3 SB Register Space</b>		
13.2.1.3#1	13.002	A Router shall support the additional registers and register fields in Table 13-5 and Table 13-6.
13.2.1.3#2	TBD	A TBT3 Router may respond to a read from Register 12 with either 2 or 3 bytes. In the case of a 2-byte response, a Router shall infer that USB4 Sideband Channel Support is 0b and TBT3-Compatible Speeds Support is 1b.
<b>13.2.1.4 Lane Initialization</b>		
<b>13.2.1.4.1 Phase 1 – Determination of Initial Conditions</b>		
13.2.1.4.1#1	IOP	A Router shall not continue on to Phase 2 until it has obtained the connection information described in this section and in Section 4.1.2.1.
13.2.1.4.1#2	IOP	If TBT3 Mode is established on the Link, a Router shall proceed with Lane Initialization as defined in Section 4.1.2 with the changes defined in this chapter.
<b>13.2.1.4.2 Phase 3 – Determination of USB4 Port Characteristics</b>		
13.2.1.4.2#1	IOP	Router shall decide the Lane attributes using the decision criteria in Table 4-18 with the changes defined in Table 13-7.
13.2.1.4.2#2	IOP	Router A shall enable RS-FEC if at least one side of the Link requests it (i.e. the RS-FEC Request (Gen 2) bit is set to 1b in the SB Register Space of the local USB4 Port and/or its Link Partner).

13.2.1.4.2#3	IOP	Otherwise, RS-FEC shall not be enabled.
13.2.1.4.2#4	IOP	Router A shall set the RS-FEC Enabled (Gen 2) bit in the USB4 Port Capability to reflect whether it is operating with RS-FEC.
13.2.1.4.2#5	TD 13.1.003	The Sideband Channel of Router A shall operate as a TBT3-Compatible Channel if any of the following are true: The USB4 Sideband Channel Support bit in the SB Register Space of one of the Routers is 0b; The Link is an Active Cable with bidirectional Re-timers.
13.2.1.4.2#6	TD 13.1.003	Else, the Sideband Channel of Router A shall operate as a USB4 Sideband Channel.
13.2.1.4.2#7	TD 13.1.003	When sending a Broadcast RT Transaction on a USB4 Sideband Channel, Router A shall set the USB4 bit to 1b.
13.2.1.4.2#8	TD 13.1.003	When sending a Broadcast RT Transaction on a TBT3-Compatible Sideband Channel, Router A shall set the USB4 bit to 0b.
<b>13.2.1.4.3 Phase 4 – Lane Parameters Synchronization and Transmit Start</b>		
13.2.1.4.3#1	TD 13.1.003	Router A shall do the following for each enabled Lane to indicate that it is ready to start transmission on a given Lane:
13.2.1.4.3#2	TD 13.1.003	If the Router Assembly for Router A does not include any On-Board Re-timers, and if operating at Gen 2 speed, Router A shall send an LT_Gen_2 Transaction for each enabled Lane every tLaneParams.
13.2.1.4.3#3	TD 13.1.003	Router A shall continue sending LT_Gen_2 Transactions until all of the following are true, then continue to Step 2: At least tLTPhase4 time has passed from completion of Phase 2; Router A has sent LT_Gen_2 Transactions at least twice; Router A has received an LT_Gen_2 Transaction from Router B.
13.2.1.4.3#4	TD 13.1.003	If the Router Assembly for Router A does not include any On-Board Re-timers, and if operating at Gen 3 speed, Router A shall send an LT_Gen_3 Transaction for each enabled Lane every tLaneParams.
13.2.1.4.3#5	TD 13.1.003	Router A shall continue sending LT_Gen_3 Transactions until all of the following are true, then continue to Step 2: At least tLTPhase4 time has passed from completion of Phase 2; Router A has sent LT_Gen_3 Transactions at least twice; Router A has received an LT_Gen_3 Transaction from Router B.
13.2.1.4.3#6	TD 13.1.003	If the Router Assembly for Router A includes one or more On-Board Re-timers, and if operating at Gen 2 speed, Router A shall send a Broadcast RT Transaction every tLaneParams.
13.2.1.4.3#7	TD 13.1.003	The Broadcast RT Transaction shall have the parameter values in Table 4-18.
13.2.1.4.3#8	TD 13.1.003	Router A shall also send an LT_Gen_2 Transaction for each enabled Lane.

13.2.1.4.3#9	TD 13.1.003	Router A shall continue sending the Broadcast RT and LT_Gen_2 Transactions until all of the following conditions are true: At least tLTPHase4 time has passed from completion of Phase 2; Router A has sent LT_Gen_2 Transactions at least twice; Router A has received an LT_Gen_2 Transaction from Router B.
13.2.1.4.3#10	TD 13.1.003	If the Router Assembly for Router A includes one or more On-Board Re-timers, and if operating at Gen 3 speed, Router A shall send a Broadcast RT Transaction every tLaneParams.
13.2.1.4.3#11	TD 13.1.003	The Broadcast RT Transaction shall have the parameter values in Table 4-18.
13.2.1.4.3#12	TD 13.1.003	Router A shall also send an LT_Gen_3 Transaction for each enabled Lane.
13.2.1.4.3#13	TD 13.1.003	Router A shall continue sending the Transactions until all of the following conditions are true: At least tLTPHase4 time has passed from completion of Phase 2; Router A has sent LT_Gen_3 Transactions at least twice; Router A has received an LT_Gen_3 Transaction from Router B.
<b>13.2.1.4.4 Phase 5 – Link Equalization</b>		
13.2.1.4.4#1	TD 13.1.003	(Transmitter) If Router A connects to an On-Board Re-timer in the same Router Assembly, then Router A's transmitter shall perform the transmitter flow in the symmetric equalization flow defined in Section 4.1.2.5.1.
13.2.1.4.4#2	TD 13.1.003	(Transmitter) If Router A connects to a Cable Re-timer: Router A's transmitter shall perform the Primary Partner flow in the Asymmetric TxFFE Parameter Negotiation with a transmitting Primary Partner defined in Section 13.2.1.4.4.1.
13.2.1.4.4#3	TD 13.1.003	(Transmitter) If Router A connects to a Cable Re-timer: Once a transmitter completes TxFFE negotiation with the Cable Re-timer's receiver, Router A shall send an LT_Resume2 Transaction on the USB4 Port that completed negotiation with the LSELane field matching the Lane number that completed negotiation.
13.2.1.4.4#4	TD 13.1.003	(Transmitter) If Router A either connects directly to Router B or connects to an On-Board Re-timer in the Router Assembly of Router B (through a Passive Cable or Cable with re-driver), then Router A's transmitter shall perform the transmitter flow in the symmetric equalization flow defined in Section 4.1.2.5.1.
13.2.1.4.4#5	TD 13.1.003	(Receiver) If Router B connects to an On-Board Re-timer, then Router B's receiver shall perform the receiver flow in the symmetric equalization flow defined in Section 4.1.2.5.1.
13.2.1.4.4#6	TD 13.1.003	(Receiver) When a receiver's equalization flow is complete on a Lane, the Router shall set the Lane's Clock Switch Done bit to 1b
13.2.1.4.4#7	TD 13.1.003	(Receiver) If Router B connects to a Cable Re-timer, then Router B's receiver shall perform the Primary Partner flow in the Asymmetric TxFFE Parameter Negotiation with a Receiving Primary Partner defined in Section 13.2.1.4.4.2.

13.2.1.4.4#8	TD 13.1.003	(Receiver) If Router B either connects directly to Router A or connects to an On-Board Re-timer in the Router Assembly of Router A, then Router B's receiver shall perform the receiver flow in the symmetric equalization flow defined in Section 4.1.2.5.1.
<b>13.2.1.4.4.1 Phase 5 – Asymmetric TxFFE Parameter Negotiation with a Transmitting Primary Partner</b>		
<b>Transmitting Primary Partner flow:</b>		
13.2.1.4.4.1#1	TD 13.1.003	1) The transmitter shall start with the TX Active bit set to 1b (default value) in the Tx Status byte of the TxFFE register
13.2.1.4.4.1#2	TD 13.1.003	2) The transmitter shall send an AT Transaction with a write Command to the receiver that sets the Tx Active bit to 1b in the Partner Tx Status byte in the TxFFE register
13.2.1.4.4.1#3	TD 13.1.003	3) The transmitter shall read the local <i>Rx Status &amp; TxFFE Request</i> byte from the receiver.
13.2.1.4.4.1#4	NT	Deprecated
13.2.1.4.4.1#5	TD 13.1.003	4) If Rx Locked = 1b, then negotiation is complete and no further TxFFE negotiation steps shall be taken.
13.2.1.4.4.1#6	TD 13.1.003	4) Else if New Request = 0b and TxFFE Request is the same as the previous TxFFE Request, the receiver has not provided a new request yet. The Router shall go to Step 3. The Router shall perform Step 3 within tPollTxFFE of receiving the AT Response.
13.2.1.4.4.1#7	TD 13.1.003	4) Else, this is a new request to update TxFFE parameters. Continue on to Step 5.
13.2.1.4.4.1#8	TD 13.1.003	5) The transmitter shall update its transmitter parameters based on the new parameters received in the AT Response
13.2.1.4.4.1#9	TD 13.1.003	5) If both Lane Adapters in the Port are enabled and have not yet completed TxFFE negotiation, both transmitters must complete Step 5 before continuing to Step 6. If the other Lane Adapter has not yet completed Step 5, the transmitter shall wait for the other Lane to finish Step 5 before continuing to Step 6.
13.2.1.4.4.1#10	TD 13.1.003	6) The transmitter shall inform the receiver that it has updated to new parameters by sending an AT Transaction with a write Command to the receiver targeting its Partner Tx Status byte in the TxFFE register with the following contents: Tx Active = 1b; TxFFE Setting = value received in Step 4.
13.2.1.4.4.1#11	TD 13.1.003	7) The transmitter shall read the local <i>Rx Status &amp; TxFFE Request</i> byte from the receiver.
13.2.1.4.4.1#12	NT	Deprecated

13.2.1.4.4.1#13	TD 13.1.003	8) If New Request = 1b and TxFFE Request is the same as the previous TxFFE Request, the Router shall return to and perform Step 7 within tPollTXFFE of receiving the AT Response.
13.2.1.4.4.1#14	TD 13.1.003	8) Else, go to Step 3.
<b>13.2.1.4.4.2 Phase 5 – Asymmetric TxFFE Parameter Negotiation with a Receiving Primary Partner</b>		
<b>Receiving Primary Partner flow:</b>		
13.2.1.4.4.2#1	TD 13.1.003	1) The receiver shall start with the following default values in the <i>Rx Status &amp; TxFFE Request</i> byte of the TxFFE register: Rx Locked = 0b; New Request bit = 0b; Rx Active bit = 0b.
13.2.1.4.4.2#2	TD 13.1.003	2) The receiver shall read the Local Tx Status byte of the transmitter.
13.2.1.4.4.2#3	TD 13.1.003	2) On reception of an AT Response from the transmitter, the receiver shall do the following: If Tx Active = 1b (i.e. the transmitter is transmitting), then enable the receiver, set Rx Active to 1b, and go to Step 3. Else, repeat Step 2 within tPollTXFFE of receiving the AT Response.
13.2.1.4.4.2#4	TD 13.1.003	3) The receiver shall evaluate its receiver behavior. If equalization is complete, the receiver shall set the Rx Locked field to 1b.
13.2.1.4.4.2#5	TD 13.1.003	4) The receiver shall do the following: If Rx Locked = 1, then go to Step 5. Else, go to Step 6
13.2.1.4.4.2#6	TD 13.1.003	5) TXFFE negotiation is complete.
13.2.1.4.4.2#7	TD 13.1.003	6) The receiver shall select a new set of TxFFE parameters.
13.2.1.4.4.2#8	TD 13.1.003	7) The receiver shall write the Partner <i>Rx Status &amp; TxFFE Request</i> byte at the transmitter as follows: If the Transmitting Primary Partner finished TxFFE on both Lanes, then the receiver sends an AT Command with a write Command targeting the Partner <i>Rx Status &amp; TxFFE Request</i> byte of the TxFFE register of the transmitter. Else, the receiver will wait for the next AT Command with a write Command to the TxFFE Register from the Transmitting Primary Partner and use it to write the Partner <i>Rx Status &amp; TxFFE Request</i> byte of the TxFFE register of the transmitter. The AT command shall write to following values to the following fields: New Request = 1b; Rx Active = 1b; TxFFE Request = index of selected set of TxFFE parameters.
13.2.1.4.4.2#9	TD 13.1.003	8) The receiver shall wait for a write Response indicating the transmitter is using the new requested TxFFE settings.
13.2.1.4.4.2#10	TD 13.1.003	9) The receiver shall evaluate its receiver behavior. If equalization is complete, the receiver shall set the Rx Locked field to 1b.

13.2.1.4.4.2#11	TD 13.1.003	10) The receiver shall write the Partner <i>Rx Status &amp; TxFFE Request</i> byte at the transmitter as follows: If the Transmitting Primary Partner finished TxFFE on both Lanes, then the receiver sends an AT Command with a write Command targeting the Partner <i>Rx Status &amp; TxFFE Request</i> byte of the TxFFE register of the transmitter.
13.2.1.4.4.2#12	TD 13.1.003	10) The receiver shall write the Partner <i>Rx Status &amp; TxFFE Request</i> byte at the transmitter as follows: Else, the receiver will wait for the next AT Command with a write Command to the TxFFE Register from the Transmitting Primary Partner and use it to write the Partner <i>Rx Status &amp; TxFFE Request</i> byte of the TxFFE register of the transmitter. The AT Command shall write to following values to the following fields: New Request = 0b; Rx Active = 1b; Rx Locked = updated value
13.2.1.4.4.2#13	TD 13.1.003	11) The receiver shall do the following: If Rx Locked = 1, then go to Step 5. Else, go to Step 6.
<b>13.2.2 Logical Layer State Machine</b>		
<b>13.2.2.1 CLd State</b>		
<b>13.2.2.1.1 Behavior in State</b>		
13.2.2.1.1#1	NT	Deprecated.
13.2.2.1.1#2	NT	Deprecated.
13.2.2.1.1#3	NT	Deprecated.
13.2.2.1.1#4	NT	Deprecated.
13.2.2.1.1#5	NT	Deprecated.
13.2.2.1.1#6	NT	Deprecated.
<b>13.2.2.2 TS1 and TS2 Ordered Sets</b>		
13.2.2.2#1	IOP	When operating in TBT3 mode, TS1 and TS2 Ordered Sets shall have the format shown in Table 4-25 with the changes in Table 13-8.
13.2.2.2#2	IOP	Lane Bonding Target 2. Transmitter shall either set this value to match the Lane Bonding Target field or shall set this value to 001b.
13.2.2.2#3	NT	Lane Bonding Target 2. A Receiver shall ignore this field.
<b>13.2.3 USB4 Link Operation</b>		
<b>13.2.3.1 USB4 Link Transitions</b>		
13.2.3.1#1	IOP	When TBT3 Mode is established on the Link, a USB4 Port shall support the transitions described in Section 4.2.2 with the following changes:

13.2.3.1#2	TD 13.1.004	For a Device Router that supports TBT3 Mode on its Upstream Facing Port, all USB4 Ports shall support operation with two Single-Lane Links.
<b>13.2.3.2 Pre-Coding</b>		
13.2.3.2#1	NT	In addition to the conditions defined in Section 4.3.6.2, Pre-Coding shall be off when the Link uses a TBT3-Compatible Sideband Channel.
<b>13.2.4 Sleep and Wake</b>		
13.2.4#1	NT	If bits 15:12 in the Connection Manager USB4 Version field in the Router Configuration Space are 0b (indicating a TBT3 Connection Manager), a Router shall support Sleep and Wake per Section 4.5 with the changes defined in this section.
<b>13.2.4.1 Entry to Sleep</b>		
13.2.4.1#1	NT	After the Enter Sleep bit is set to 1b in all Ports, a Device Router shall do the following for each USB4 Port: Transition the USB4 Adapters to CLd state.
13.2.4.1#2	NT	After the Enter Sleep bit is set to 1b in all Ports, a Device Router shall do the following for each USB4 Port: If any of the following conditions apply, the USB4 Port shall go through disconnect: For Lane 0 in a USB4 Port: The Lane 0 is Inter-Domain bit is 0b and the Lane 0 Configured bit is 0b; The Lane 0 is Inter-Domain bit is 1b and the Inter-Domain Disconnect on Sleep bit is set to 1b.
13.2.4.1#3	NT	Deprecated.
<b>13.2.4.2 Behavior in Sleep State</b>		
13.2.4.2#1	NT	A Device Router shall retain a copy of the state information listed in Table 13-9 separate from Configuration Space.
13.2.4.2#2	NT	If the USB4 Port is disconnected while in Sleep state, then the internal Lane 0 is Inter-Domain state, Lane 0 Configured state, <i>Lane 1 is Inter-Domain state</i> , and <i>Lane1 Configured</i> state listed in Table 13-9 shall all transition to 0b.
13.2.4.2#3	NT	Deprecated.
<b>13.2.4.3 Wake Events</b>		
13.2.4.3#1	NT	A Device Router shall support all of the wake events listed in the Enable Wake Events field of the USB4 Port Region in the Vendor Specific Extended 6 Capability of the Router Configuration Space.
<b>13.2.4.4 Exit From Sleep</b>		
13.2.4.4#1	NT	A Device Router shall not start Lane Initialization for Lane 0 until the Start Link Initialization bit is set to 1b, if either of the following is true on exit from sleep: The Lane 0 Configured state is set to 0b; The Lane 0 is Inter-Domain bit is 1b.



13.2.4.4#2	NT	A Device Router shall not start Lane Initialization for Lane 1 until the Start Link Initialization bit is set to 1b, if either of the following is true on exit from sleep: The Lane 1 Configured state is set to 0b; The Lane 1 is Inter-Domain bit is 1b.
<b>13.2.5 Timing Parameters</b>		

## Ver. 2 Router Assertions

### Chapter 4

The following Table presents the USB4 Ver. 2 Specification Chapter 4 asserts.

Assertion #	Test Name	Assertion Description
<b>4 Logical Layer</b>		
<b>4.1 Sideband Channel</b>		
<b>4.1.1 Transactions</b>		
<b>4.1.1.1 Symbols</b>		
4.1.1.1#1	IOP	A Sideband Channel shall encode all transmitted Symbols using the 10-bit Start/Stop encoding scheme as follows: A Start bit (logical 0b), Eight bits of payload, and A Stop bit (logical 1b).
<b>4.1.1.2 Transaction Types</b>		
4.1.1.2#1	IOP	The symbols within a transaction shall be sent in ascending order.
4.1.1.2#2	IOP	The bits within a symbol shall be sent in the order from bit 0 to bit 7.
<b>4.1.1.2.1 LT Transactions</b>		
4.1.1.2.1#1	BC	An LT Transaction shall consist of the three Symbols described in Table 4-1.
4.1.1.2.1#2	NT	Within a LSE Symbol: Bit 5 (LSELane) shall be 0b (for Lane 0) or 1b (for Lane 1).
4.1.1.2.1#3	BC	Within a LSE Symbol: Bit 5 (LSELane) shall be set to 0b when issuing an LT_LRoff Transaction.
4.1.1.2.1#4	BC	Within a LSE Symbol: Bits [7:6] (StartLT) shall be set to 10b.
4.1.1.2.1#5	0	The recipient of an LT Transaction shall verify that the CLSE Symbol payload is a bitwise complement of the LSE Symbol payload.
4.1.1.2.1#6	0	An LT Transaction that fails this check shall be dropped and no further action shall be taken on its behalf.
<b>4.1.1.2.2 AT Transactions</b>		
4.1.1.2.2#1	BC	An AT Transaction shall consist of the Symbols in Table 4-3.
4.1.1.2.2#2	BC	The number of Data Symbols (n) in an AT Transaction shall not exceed 66.
4.1.1.2.2#3	NT	Within a STX Symbol for an AT Transaction: Bit 0 ( <i>CmdNotResp</i> ) shall be set to 0b for an AT Response or 1b for an AT Command.

4.1.1.2.2#4	BC	Within a STX Symbol: Bit 1 ( <i>ReturnBounce</i> ) shall be set to 0b.
4.1.1.2.2#5	BC	Within a STX Symbol for an AT Transaction: Bit 2 ( <i>Recipient</i> ) shall be set to 1b.
4.1.1.2.2#6	BC	Within a STX Symbol for an AT Transaction: Bit 3 ( <i>Bounce</i> ) shall be set to 0b.
4.1.1.2.2#7	BC	Within a STX Symbol for an AT Transaction: Bit 4 ( <i>Responder</i> ) shall be set to 0b.
4.1.1.2.2#8	BC	Within a STX Symbol for an AT Transaction: Bits [7:6] ( <i>StartAT</i> ) shall be set to 00b.
4.1.1.2.2#9	BC	A Router that receives an AT Command with the Recipient bit set to 1b shall respond with an AT Response.
<b>4.1.1.2.3 RT Transactions</b>		
<b>4.1.1.2.3.1 Broadcast RT Transaction</b>		
4.1.1.2.3.1#1	BC	A Broadcast RT Transaction shall have the format shown in Table 4-5.
4.1.1.2.3.1#2	NT	Within a STX Symbol for a Broadcast RT Transaction: Bits [7:6] ( <i>StartRT</i> ) shall be set to 01b.
4.1.1.2.3.1#3	NT	Within a STX Symbol for a Broadcast RT Transaction: Bit 5 ( <i>Broadcast</i> ) shall be set to 1b.
4.1.1.2.3.1#4	BC TD 4.005	Within a STX Symbol for a Broadcast RT Transaction: Bits [4:1] ( <i>Index</i> ) shall be set to 0.
4.1.1.2.3.1#5	BC	Within a STX Symbol for a Broadcast RT Transaction: Bit 0 ( <i>CmdNotResp</i> ) shall be set to 1b.
4.1.1.2.3.1#6	BC	Within Byte 2 of a Broadcast RT Transaction: Bit 4 ( <i>TBT3-Compatible Speed</i> ) is set to 0b.
4.1.1.2.3.1#7	BC	Within Byte 2 of a Broadcast RT Transaction: Bit 0 ( <i>USB4</i> ) is set to 1b.
4.1.1.2.3.1#8	TD 4.005	Within Byte 3 of a Broadcast RT Transaction: Bit 1 ( <i>Lane1Enabled</i> ) shall equal the value of the Enabling Decision (Lane 1) bit in the Link Configuration register of the SB Register Space.
4.1.1.2.3.1#9	TD 4.005	Within Byte 3 of a Broadcast RT Transaction: Bit 0 ( <i>Lane0Enabled</i> ) shall equal the value of the Enabling Decision (Lane 0) bit in the Link Configuration register of the SB Register Space.

<b>4.1.1.2.3.2 Addressed RT Transaction</b>		
4.1.1.2.3.2#1	BC	An Addressed RT Transaction shall have the format shown in Table 4-9.
4.1.1.2.3.2#2	BC	The number of Data Symbols shall not exceed 66.
4.1.1.2.3.2#3	NT	Within a STX Symbol for an Addressed RT Transaction: Bits [7:6] ( <i>StartRT</i> ) shall be set to 01b.
4.1.1.2.3.2#4	NT	Within a STX Symbol for an Addressed RT Transaction: Bit 5 ( <i>Broadcast</i> ) shall be set to 0b.
4.1.1.2.3.2#5	NT	Within a STX Symbol for an Addressed RT Transaction: Bits [4:1] ( <i>Index</i> ) in an Addressed RT Command shall be set to 0 if the target of the Transaction is the first Router or Re-timer that receives the Transaction.
4.1.1.2.3.2#6	NT	Else, shall be set to the Re-timer Index of the Re-timer that is the target of the Command.
4.1.1.2.3.2#7	NT	Within a STX Symbol for an Addressed RT Transaction: Bit 0 ( <i>CmdNotResp</i> ) shall be set to 0b for an Addressed RT Response or 1b for an Addressed RT Command.
4.1.1.2.3.2#8	NT	A Router that receives an Addressed RT Command with the Index field set to 0 shall respond with an Addressed RT Response.
4.1.1.2.3.2#9	TD 4.001	A Router shall not respond to Addressed RT Commands with a non-zero Index field.
<b>4.1.1.2.4 AT and RT Transaction Rules</b>		
4.1.1.2.4#1	NT	A transmitter shall not abort an AT Transaction or an RT Transaction after the STX Symbol is sent.
4.1.1.2.4#2	TD 4.028	When a receiver receives two or more leading DLE symbols it shall discard the extra leading DLE symbols and process the received LT Transaction as if only one leading DLE symbol was received
4.1.1.2.4#3	TD 4.002	If any Data Symbol or a CRC Symbol in an AT Transaction or an RT Transaction contains the same payload as a DLE Symbol, the transmitter of the AT Transaction or RT Transaction shall insert a Symbol with payload of FEh in front of that Data Symbol.
4.1.1.2.4#4	TD 4.002	The recipient of an AT Transaction or an RT Transaction shall strip all duplicating FEh Symbols that immediately precede a Data Symbol or a CRC Symbol.
4.1.1.2.4#5	BC	Each AT Transaction or RT Transaction shall include a 16-bit CRC.
4.1.1.2.4#6	BC	Only the STX and Data Symbols shall be used in CRC calculation.

4.1.1.2.4#7	BC	The CRC shall be calculated in increasing Symbol order, starting with the STX Symbol.
4.1.1.2.4#8	BC	Within each Symbol, CRC shall be calculated from bit[7] to bit[0].
4.1.1.2.4#9	BC	The CRC shall be calculated using the following rules: Width: 16; Poly: 8005h; Init: FFFFh; RefIn: True; RefOut: True; XorOut: 0000h.
<b>4.1.1.2.5 AT and RT Command Rules</b>		
4.1.1.2.5#1	IOP	A Router shall process AT Commands and AT Responses arriving from the Link Partner or Re-timer in the order received.
4.1.1.2.5#2	IOP	A Router shall process Addressed RT Commands and Addressed RT Responses arriving from a Re-timer in the order received.
4.1.1.2.5#3	TD 4.004	A Router shall not send an AT Command or Addressed RT Command while it is waiting for a response for either a previously sent AT Command or a previously sent Addressed RT Command.
<b>4.1.1.2.5.1 AT Commands</b>		
4.1.1.2.5.1#1	BC	The recipient of an AT Command shall send an AT Response within tCmdResponse of receiving the AT Command.
4.1.1.2.5.1#2	NT	If a Router sends an AT Command, then receives at least two AT Commands from the target of the outstanding AT Command within tATTimeout, it shall stop waiting for an AT Response and shall immediately reissue the outstanding AT Command.
4.1.1.2.5.1#3	TD 4.004	Otherwise, a Router shall wait tATTimeout for an AT Response.
<b>4.1.1.2.5.2 Addressed RT Commands</b>		
4.1.1.2.5.2#1	BC	The recipient of an Addressed RT Command shall send an Addressed RT Response within tCmdResponse of receiving the Addressed RT Command.
4.1.1.2.5.2#2	TD 4.004	A Router shall wait tRTTimeout for an Addressed RT Response.
<b>4.1.1.2.6 Receiver Decoding of LT, AT, and RT Transactions</b>		
4.1.1.2.6#1	TD 4.029	A Router shall ignore and discard an AT Transaction or an Addressed RT Transaction if any of the following are true: The CRC in the Transaction is invalid.
4.1.1.2.6#2	TD 4.029	A Router shall ignore and discard an AT Transaction or an Addressed RT Transaction if any of the following are true: The Transaction has no data and no CRC field.
4.1.1.2.6#3	TD 4.029	Any sequence of Symbols not handled as an LT Transaction, an AT Transaction, or an RT Transaction shall be discarded.

4.1.1.2.6#4	TD 4.029	An AT Response or an RT Response shall not be sent in response to such a sequence.
<b>4.1.1.3 SB Register Space</b>		
4.1.1.3#1	NT	A Router shall maintain one SB Register Space per USB4 Port.
<b>4.1.1.3.1 Router Access</b>		
4.1.1.3.1#1	BC	An AT Command or RT Command shall consist of the Symbols described in Table 4-12.
4.1.1.3.1#2	BC	In an AT or RT Command, LEN shall not be greater than 64.
4.1.1.3.1#3	IOP	For a Write Command, COMMAND_DATA register Contents shall appear least significant byte first.
4.1.1.3.1#4	BC	An AT Response or RT Response shall consist of the Symbols described in Table 4-13.
4.1.1.3.1#5	IOP	For a Read Response, RESPONSE_DATA register contents shall appear low-ordered byte first.
4.1.1.3.1#6	TD 4.030	When a Router receives an AT Command or an RT Command, it shall process the AT or RT Command according to Table 4-14 and in the order listed: Operation with a single Data Symbol, send a Response with no RESPONSE_DATA and LEN set to 0.
4.1.1.3.1#7	TD 4.030	When a Router receives an AT Command or an RT Command, it shall process the AT or RT Command according to Table 4-14 and in the order listed: Read operation to an unsupported vendor defined register or to an undefined register, send a Response with no RESPONSE_DATA and LEN set to 0.
4.1.1.3.1#8	TD 4.030	When a Router receives an AT Command or an RT Command, it shall process the AT or RT Command according to Table 4-14 and in the order listed: Read operation with more than two Data Symbols, send a Response with no RESPONSE_DATA and LEN set to 0.
4.1.1.3.1#9	TD 4.030	When a Router receives an AT Command or an RT Command, it shall process the AT or RT Command according to Table 4-14 and in the order listed: Read operation of more bytes than the target register length, send a Response with the entire register contents in the RESPONSE_DATA and LEN set to the number of bytes in the RESPONSE_DATA field.
4.1.1.3.1#10	TD 4.030	When a Router receives an AT Command or an RT Command, it shall process the AT or RT Command according to Table 4-14 and in the order listed: Read operation of fewer bytes than the target register length, send a Response with the number of bytes requested in the RESPONSE_DATA and LEN set to the number of bytes in the RESPONSE_DATA field.

4.1.1.3.1#11	IOP	When a Router receives an AT Command or an RT Command, it shall process the AT or RT Command according to Table 4-14 and in the order listed: All other read operations, perform the Read Command and send a Read Response with the contents of the register being accessed in the RESPONSE_DATA field.
4.1.1.3.1#12	TD 4.003	When a Router receives an AT Command or an RT Command, it shall process the AT or RT Command according to Table 4-14 and in the order listed: Write operation to an unsupported vendor defined register or to an undefined register, do not perform the Write Command, send a Response with the LEN field = 0 and the Result Code = 01h (ERROR) in the RESPONSE_DATA field.
4.1.1.3.1#13	TD 4.003	When a Router receives an AT Command or an RT Command, it shall process the AT or RT Command according to Table 4-14 and in the order listed: Write operation with LEN field that does not match the Transaction size, do not perform the Write Command, send a Response with the LEN field = 0 and the Result Code = 01h (ERROR) in the RESPONSE_DATA field.
4.1.1.3.1#14	TD 4.003	When a Router receives an AT Command or an RT Command, it shall process the AT or RT Command according to Table 4-14 and in the order listed: Write operation to a Read-only (RO) register, do not perform the Write Command, a send a Response with the LEN field = 0 and the Result Code = 01h (ERROR) in the RESPONSE_DATA field.
4.1.1.3.1#15	TD 4.003	When a Router receives an AT Command or an RT Command, it shall process the AT or RT Command according to Table 4-14 and in the order listed: Write operation of more bytes than the target register length, do not perform the Write Command, send a Response with the LEN field = 0 and the Result Code = 01h (ERROR) in the RESPONSE_DATA field.
4.1.1.3.1#16	TD 4.003	When a Router receives an AT Command or an RT Command, it shall process the AT or RT Command according to Table 4-14 and in the order listed: Write operation of less bytes than the target register length, perform the write operation only on the requested bytes, send a Response with the LEN field equal to the size in bytes of the register being accessed and the Result Code = 00h (SUCCESS) in the RESPONSE_DATA field.
4.1.1.3.1#17	IOP	When a Router receives an AT Command or an RT Command, it shall process the AT or RT Command according to Table 4-14 and in the order listed: All other write operations, perform the Write Command and send a Response with the LEN field equal to the size in bytes of the register being accessed and the Result Code = 00h (SUCCESS) in the RESPONSE_DATA field.
<b>4.1.1.3.2 Connection Manager Access</b>		
4.1.1.3.2#1	NT	When the <i>Pending</i> bit in a USB4 Port Capability is set to 1b, a Router shall: If the <i>Target</i> field in the USB4 Port Capability is set to 000b, the Router shall issue an access to the SB Register Space of the Port.
4.1.1.3.2#2	NT	The Router shall access the register identified in the <i>Address</i> field in the USB4 Port Capability.

4.1.1.3.2#3	NT	The Router shall access the number of bytes indicated in the <i>Length</i> field.
4.1.1.3.2#4	NT	If the <i>WnR</i> field is set to 0b, the Router shall read from the SB Register Space.
4.1.1.3.2#5	NT	If the <i>WnR</i> field is set to 1b, the Router shall write to the SB Register Space.
4.1.1.3.2#6	NT	The Router shall write the contents from the <i>Data</i> DWs in the USB4 Port Capability.
4.1.1.3.2#7	NT	Register contents shall be written least significant byte first.
4.1.1.3.2#8	NT	When the <i>Pending</i> bit in a USB4 Port Capability is set to 1b, a Router shall: If the <i>Target</i> field in the USB4 Port Capability is set to 001b, the Router shall send an AT Command on the Sideband Channel of the Port to access the SB Register Space of the Link Partner.
4.1.1.3.2#9	NT	The AT Command shall have the following contents: The <i>REG</i> field shall be set to the contents of the <i>Address</i> field in the USB4 Port Capability.
4.1.1.3.2#10	NT	The AT Command shall have the following contents: The <i>LEN</i> field shall be set to the contents of the <i>Length</i> field in the USB4 Port Capability.
4.1.1.3.2#11	NT	The AT Command shall have the following contents: The <i>WnR</i> field shall be set to the contents of the <i>WnR</i> field in the USB4 Port Capability.
4.1.1.3.2#12	NT	The AT Command shall have the following contents: If the <i>WnR</i> field is set to 1b, the COMMAND DATA Symbols shall contain the contents from the <i>Data</i> DWs in the USB4 Port Capability. Register contents shall appear least significant byte first.
4.1.1.3.2#13	NT	When the <i>Pending</i> bit in a USB4 Port Capability is set to 1b, a Router shall: If the <i>Target</i> field in the USB4 Port Capability is set to 010b, the Router shall send an Addressed RT Command on the Sideband Channel of the Port to access the SB Register Space of a Re-timer on the Link.
4.1.1.3.2#14	NT	The Addressed RT Command shall have the following contents: The <i>Index</i> field in an Addressed RT Command shall be set to the contents of the Re-timer Index in the USB4 Port Capability.
4.1.1.3.2#15	NT	The Addressed RT Command shall have the following contents: The <i>REG</i> field in an Addressed RT Command shall be set to the contents of the <i>Address</i> field in the USB4 Port Capability.
4.1.1.3.2#16	NT	The Addressed RT Command shall have the following contents: The <i>LEN</i> field in an Addressed RT Command shall be set to the contents of the <i>Length</i> field in the USB4 Port Capability.
4.1.1.3.2#17	NT	The Addressed RT Command shall have the following contents: The <i>WnR</i> field in an Addressed RT Command shall be set to the contents of the <i>WnR</i> field in the USB4 Port Capability.



4.1.1.3.2#18	NT	The Addressed RT Command shall have the following contents: If the <i>WnR</i> field in an Addressed RT Command is set to 1b, the <i>COMMAND_DATA</i> Symbols shall contain the contents from the <i>Data</i> DWs in the USB4 Port Capability. Register contents shall appear least significant byte first.
4.1.1.3.2#19	NT	A Router shall process an AT Command as described in Table 4-14.
4.1.1.3.2#20	TD 4.004	When a response to a local access is ready or when a Response Transaction is received, the Router shall update the USB4 Port Capability as follows: The <i>LEN</i> field in the AT Response, the RT Response, or the local access is copied to the <i>Length</i> field in the USB4 Port Capability.
4.1.1.3.2#21	TD 4.004	When a response to a local access is ready or when a Response Transaction is received, the Router shall update the USB4 Port Capability as follows: The <i>No Response</i> bit is updated.
4.1.1.3.2#22	TD 4.004	When a response to a local access is ready or when a Response Transaction is received, the Router shall update the USB4 Port Capability as follows: The <i>Result Code</i> bit in the USB4 Port Capability is updated.
4.1.1.3.2#23	NT	When a response to a local access is ready or when a Response Transaction is received, the Router shall update the USB4 Port Capability as follows: For a read, the <i>Data</i> DWs in the USB4 Port Capability are updated.
4.1.1.3.2#24	TD 4.004	The Router shall then set the <i>Pending</i> bit in the USB4 Port Capability to 0b.
<b>4.1.1.3.3 SB Register Definitions</b>		
4.1.1.3.3#1	TD 4.003	A Write operation to a field with the RO access type shall have no effect.
4.1.1.3.3#2	NT	A Read operation to a field with the RO access type shall return a meaningful value.
4.1.1.3.3#3	NT	A field with the RW access type shall be capable of both Read operation and Write operation.
4.1.1.3.3#4	NT	The value read from a field with RW access type shall reflect the last value written to it unless the field was reset in the interim.
4.1.1.3.3#5	NT	A Write operation to a Rsvd field shall have no effect.
4.1.1.3.3#6	TD 4.005	The SB Register Space registers shall have the structure and fields described in Table 4-17.
4.1.1.3.3#7	NT	Registers not listed in Table 4-17 are undefined and shall not be used.
4.1.1.3.3#8	TD 4.005	The Vendor ID Low field shall contain the same value as the lower byte of the Vendor ID field in Router Configuration Space.
4.1.1.3.3#9	TD 4.005	The Vendor ID High field shall contain the same value as the higher byte of the Vendor ID field in Router Configuration Space.

4.1.1.3.3#10	TD 4.005	The Product ID Low field shall contain the same value as the lower byte of the Device ID field in Router Configuration Space.
4.1.1.3.3#11	TD 4.005	The Product ID High field shall contain the same value as the higher byte of the Device ID field in Router Configuration Space.
4.1.1.3.3#12	CH8	A Router shall write the Completion Metadata (if any) to the Metadata field after executing a Port Operation.
4.1.1.3.3#13	TD 4.005	The Enabling Decision (Lane 0) field shall indicate whether or not Lane 0 is enabled during Lane Initialization: 0b = Adapter is in CLd state and 1b = Lane is Enabled.
4.1.1.3.3#14	TD 4.005	The Enabling Decision (Lane 1) field shall indicate whether or not Lane 1 is enabled during Lane Initialization: 0b = Adapter is in CLd state and 1b = Lane is Enabled.
4.1.1.3.3#15	TD 4.005	A Router shall set the Enabling Request (Lane 0) bit to 0b when the Lane Disable bit in the USB4 Adapter Configuration Capability for Lane 0 is 1b.
4.1.1.3.3#16	NT	A Lane 1 Adapter shall not request enabling unless the Lane 0 Adapter requests enabling.
4.1.1.3.3#17	NT	A USB4 Port shall only set the Enabling Request (Lane 1) bit to 1b if all On-Board Re-timers connected between the Router and the cable support dual Lanes.
4.1.1.3.3#18	NT	A Router shall set the Enabling Request (Lane 1) bit to 0b when the Lane Disable bit in the USB4 Adapter Configuration Capability for Lane 1 is 1b.
4.1.1.3.3#19	NT	A USB4 Port shall only set the <i>Gen 3 Support</i> bit to 1b if all of the following are true: The Port supports Gen 3 speeds; All On-Board Re-timers connected between the Port and the cable support Gen 3 speeds; The Port implements both a Lane 0 Adapter and a Lane 1 Adapter; The Target Link Speed field in the Lane Adapter Configuration Capability is 1100b.
4.1.1.3.3#20	NT	Otherwise the <i>Gen 3 Support</i> bit shall be 0b.
4.1.1.3.3#21	NT	A USB4 Port shall set the RS-FEC Request (Gen 2) bit to the same value as the Request RS-FEC Gen 2 bit in the USB4 Port Capability.
4.1.1.3.3#22	NT	A USB4 Port shall set the RS-FEC Request (Gen 3) bit to the same value as the Request RS-FEC Gen 3 bit in the USB4 Port Capability.
4.1.1.3.3#23	TD 4.005	The USB4 Sideband Channel field shall be set to 1b.
4.1.1.3.3#24	TD 4.005	A USB4 Port shall only set the TBT3-Compatible Speeds Supported bit to 1b if all On-Board Re-timers connected between the Router and the cable support TBT3-compatible speeds.
4.1.1.3.3#25	TD 4.005	Bit 2 through 7 of byte 2 in the Link Configuration register are 0 (reserved).

4.1.1.3.3#26	TD 4.005	The <i>Clock Switch Done (Lane 0)</i> bit shall be set to the value of the Rx Locked (Lane 0) bit.
4.1.1.3.3#27	TD 4.005	The <i>Clock Switch Done (Lane 1)</i> bit shall be set to the value of the Rx Locked (Lane 1) bit.
4.1.1.3.3#28	CH8	A Router shall write the Completion Data (if any) to the <i>Data</i> field after executing a Port Operation.
<b>4.1.2 Lane Initialization</b>		
4.1.2#1	IOP	The Sideband Channel shall initialize each Lane independently.
4.1.2#2	IOP	Initialization shall occur for all enabled USB4 Ports on a Router.
<b>4.1.2.1 Phase 1 – Determination of Initial Conditions</b>		
4.1.2.1#1	NT	A USB4 Port shall not continue on to Phase 2 until it has obtained the connection information described in this section.
4.1.2.1#2	NT	A USB4 Port shall not proceed to Phase 2 if the Link is not USB4.
4.1.2.1#3	NT	A USB4 Port shall drive SBTX to logic low by default.
<b>4.1.2.1.1 Lane Reversal</b>		
4.1.2.1.1#1	IOP	When a Router detects a reverse insertion on a USB Type-C connector, it shall perform Lane Reversal in the USB4 Port that faces the reversed connector.
4.1.2.1.1#2	IOP	Lane Reversal shall be performed during phase 1.
4.1.2.1.1#3	IOP	The Router shall swap the designation of Lane 0 and Lane 1 and shall associate the Lane 0 Adapter with the updated Lane 0 and the Lane 1 Adapter with the updated Lane 1.
4.1.2.1.1#4	IOP	If there are no On-Board Re-timers between Router and the USB Type-C connector, the Router shall swap its SBTX and SBRX lines facing the connector.
<b>4.1.2.1.2 Polarity Inversion</b>		
<b>4.1.2.2 Phase 2 – Router Detection</b>		
4.1.2.2#1	TD 4.005	After completion of phase 1, a Host Router shall initiate Router detection by driving SBTX to logic high on all of its Downstream Facing Ports.
4.1.2.2#2	TD 4.005	When a Device Router detects a logic high on SBRX of its Upstream Facing Port for tConnectRx time, it shall drive SBTX to logic high on all of its USB4 Ports.

4.1.2.2#3	NT	After a USB4 Port drives its SBTX to logic high and detects a logic high on its SBRX for tConnectRx time, it shall set its <i>Link Initialization in Progress</i> bit to 1b, then transition to Phase 3 of Lane Initialization.
<b>4.1.2.3 Phase 3 – Determination of USB4 Port Characteristics</b>		
4.1.2.3#1	TD 4.005	During phase 3, Router A shall read the Link Configuration Register (register 12) of Router B using AT Transactions.
4.1.2.3#2	TD 4.005	Router A shall issue at least one more register read to Router B in order to avoid a tATTimeout delay at the Link Partner.
4.1.2.3#3	NT	(Enabling) If Enabling Request = 1b in the SB Register Space of the Ports of both Router A and Router B, Router A shall: proceed to initialize the Lane.
4.1.2.3#4	TD 4.005	(Enabling) If Enabling Request = 1b in the SB Register Space of the Ports of both Router A and Router B, Router A shall: set the local Enabling Decision bit for the Lane to 1b.
4.1.2.3#5	TD 4.005	(Enabling) Else, Router A shall not initialize the Lane. The Lane shall remain in CLd state.
4.1.2.3#6	TD 4.005	(Enabling) Else, Router A shall set the local Enabling Decision bit for the Lane to 0b.
4.1.2.3#7	TD 4.005	(Dual-Lane) Router A shall set the Bonding Enabled bit in the USB4 Port Capability to 1b if all of the following are true: The USB4 Ports of Router A and Router B both have the Enabling Request bit set to 1b for both Lanes of the USB4 Port; The USB4 Ports of Router A and Router B both support Lane bonding (i.e. the Bonding Support bit is 1b in the SB Register Space of the Ports on both sides of the Lane).
4.1.2.3#8	TD 4.005	(Dual-Lane) Otherwise, Router A shall set Bonding Enabled bit to 0b.
4.1.2.3#9	IOP	(Speed) Router A shall operate at Gen 3 Lane speed if all of the following are true: The Ports on both sides of the Lane support Gen 3 ( <i>Gen 3 Support</i> is set to 1b); The cable over which Router A and Router B are communicating supports Gen 3.
4.1.2.3#10	IOP	(Speed) Otherwise, Router A shall operate at Gen 2 Lane Speed.
4.1.2.3#11	TD 4.005	(Speed) Router A shall set the Current Link Speed field in the USB4 Adapter Configuration Capability to reflect whether it is operating at Gen 2 or Gen 3 Lane speed.
4.1.2.3#12	IOP	(RS-FEC) At Gen 2 speed, Router A shall enable RS-FEC if both sides of the Link request it (i.e. the <i>RS-FEC Request (Gen 2)</i> bit is set to 1b in the SB Register Space of both the local USB4 Port and its Link Partner).
4.1.2.3#13	IOP	(RS-FEC) Otherwise, RS-FEC shall not be enabled.
4.1.2.3#14	TD 4.005	(RS-FEC) For Gen 2 speed, Router A shall set the RS-FEC Enabled (Gen 2) bit in the USB4 Port Capability to reflect whether it is operating with RS-FEC.

4.1.2.3#15	IOP	(RS-FEC) For Gen 3 speed, shall enable RS-FEC if both sides of the Link request it (i.e. the <i>RS-FEC Request (Gen 3)</i> bit is set to 1b in the SB Register Space of both the local USB4 Port and its Link Partner).
4.1.2.3#16	IOP	(RS-FEC) Otherwise, RS-FEC shall not be enabled.
4.1.2.3#17	TD 4.005	(RS-FEC) For Gen 3 speed, Router A shall set the RS-FEC Enabled (Gen 3) bit in the USB4 Port Capability to reflect whether it is operating with RS-FEC.
<b>4.1.2.4 Phase 4 – Lane Parameters Synchronization and Transmit Start</b>		
4.1.2.4#1	TD 4.005 TD 4.031	(Step 1) Router A shall send a Broadcast RT Transaction every tLaneParams with the parameter values in Table 4-18.
4.1.2.4#2	TD 4.005 TD 4.031	(Step 1) Router A shall continue sending Broadcast RT Transactions until all of the following conditions are true, then continue to step 2): At least tLTPhase4 time has passed from completion of Phase 2; Router A has sent Broadcast RT Transactions at least twice; Router A has received a Broadcast RT Transaction from Router B.
4.1.2.4#3	TD 4.005	(Step 2) Router A shall activate the transmitter on each enabled Lane at the selected speed and shall send SLOS1.
4.1.2.4#4	TD 4.005	(Step 3) After its transmitter is transmitting a valid signal, Router A shall then send an LT_Resume Transaction for each enabled Lane in the USB4 Port and shall set to 1b the Tx Active bit in the Tx Status byte of the TxFFE Register in the SB Register Space to indicate that it has started transmission on the target Lane.
4.1.2.4#5	TD 4.005	(Step 3) The LSELane field in the LT_Resume Transaction shall equal the Lane number associated with the transmitter.
<b>4.1.2.5 Phase 5 – Link Equalization</b>		
4.1.2.5#1	TD 4.005	Router A's transmitter shall perform the transmitter flow in the symmetric equalization flow defined in Section 4.1.2.5.1.1.
4.1.2.5#2	TD 4.005	A Router shall use Addressed RT Transactions with the <i>Index</i> field set to 0 to access the SB Register Space of the adjacent component, which can be either an On-Board Re-timer, a Cable Re-timer, or Router B.
4.1.2.5#3	TD 4.005	Router B's receiver shall perform the receiver flow in the symmetric equalization flow defined in Section 4.1.2.5.1.2.
4.1.2.5#4	TD 4.005	The Router shall use Addressed RT Transactions with the <i>Index</i> field set to 0b to access the SB Register Space of the adjacent component, which can be either an On-Board Re-timer, a Cable Re-timer, or Router A.
4.1.2.5#5	TD 4.005	A Router shall set the Clock Switch Done bit to 1b in the SB Register space of the Ports of a USB4 Port after all of the USB4 Port's receivers complete the equalization flow.

<b>4.1.2.5.1 Phase 5 – Symmetric TxFFE Negotiation</b>		
<b>4.1.2.5.1.1 Phase 5 – Transmitter Flow</b>		
4.1.2.5.1.1#1	NT	(Step 1) The transmitter shall start with the following default values in the Tx Status byte of the TxFFE register: Tx Active bit = 1b; Request Done bit = 0b.
4.1.2.5.1.1#2	TD 4.005	(Step 2) The transmitter shall read the <i>Rx Status &amp; TxFFE Request</i> byte of the receiver.
4.1.2.5.1.1#3	TD 4.005	(Step 3) On reception of a Response from the receiver, The transmitter shall do the following: If Rx Locked = 1, then negotiation is complete and no further TxFFE negotiation steps are taken; Else, if New Request = 0, the receiver has not provided a new request yet. The transmitter shall retry step 2 within tPollTXFFE of receiving the Response; Else, this is a new request to update TxFFE parameters. Continue on to step 4.
4.1.2.5.1.1#4	TD 4.005	(Step 4) The transmitter shall update its transmitter parameters based on the new parameters in the received Response.
4.1.2.5.1.1#5	TD 4.005	(Step 4) The transmitter shall update its Tx Status byte with the following values: TxFFE Setting = the index (from 16 possible values) loaded above to the TxFFE configuration configured at the transmitter; Request Done = 1b.
4.1.2.5.1.1#6	TD 4.005	(Step 5) The transmitter shall read the <i>Rx Status &amp; TxFFE Request</i> byte of the receiver.
4.1.2.5.1.1#7	TD 4.005	(Step 6) On reception of a Response from the receiver, the transmitter shall do the following: If New Request = 1, the receiver is still trying to lock on a previous request. The transmitter shall retry step 5 within tPollTXFFE of receiving the Response; Else, the transmitter shall set the Request Done bit in the Tx Status byte to 0b, and return to step 2.
<b>4.1.2.5.1.2 Phase 5 – Receiver Flow</b>		
4.1.2.5.1.2#1	NT	(Step 1) The receiver shall start with the following default values in the <i>Rx Status &amp; TxFFE Request</i> byte of the TxFFE register: Rx Locked bit = 0b; New Request bit = 1b; Rx Active bit = 0b.
4.1.2.5.1.2#2	TD 4.005	(Step 2) The receiver shall read the transmitter's Tx Status byte.
4.1.2.5.1.2#3	TD 4.005	(Step 3) On reception of a Response from the transmitter, the receiver shall do the following: If Tx Active = 1b, then enable the receiver, set Rx Active to 1b, and continue on to Step 4; Else, repeat step 2 within tPollTXFFE of receiving the Response.
4.1.2.5.1.2#4	TD 4.005	(Step 4) The receiver shall evaluate its receiver behavior and shall set the Rx Locked bit to 1b if equalization is complete.
4.1.2.5.1.2#5	TD 4.005	(Step 5) The receiver shall do the following: If Rx Locked = 1, then TXFFE negotiation is complete and no further negotiation steps are taken.

4.1.2.5.1.2#6	TD 4.005	(Step 5) The receiver shall do the following: If Rx Locked = 0, the receiver shall: Select a new set of TxFFE parameters and set the TxFFE Request field to the index of the selected set of TXFFE parameters; Set the New Request bit to 1b; Continue with the steps below.
4.1.2.5.1.2#7	TD 4.005	(Step 6) The receiver shall read the transmitter's Tx Status byte.
4.1.2.5.1.2#8	TD 4.005	(Step 7) On reception of a Response from the transmitter, the receiver shall do the following: If (Tx Active = 1b) AND (Request Done = 1b) AND (TxFFE Setting = value of TxFFE request in the local <i>Rx Status &amp; TxFFE Request</i> byte), then continue on to Step 8.
4.1.2.5.1.2#9	TD 4.005	(Step 7) On reception of a Response from the transmitter, the receiver shall do the following: If (Tx Active = 0b) OR (Request Done = 0b) OR (TxFFE Setting != value of TxFFE request in the local <i>Rx Status &amp; TxFFE Request</i> byte), repeat step 5 within tPollTXFFE of receiving the Response.
4.1.2.5.1.2#10	NT	(Step 8) The receiver shall evaluate its receiver behavior and set the Rx Locked bit to 1b if equalization is complete.
4.1.2.5.1.2#11	TD 4.005	(Step 9) The receiver shall set the New Request bit to 0b.
4.1.2.5.1.2#12	TD 4.005	(Step 10) The receiver shall read the transmitter's Tx Status byte by sending a read Command to the transmitter that targets its TxFFE register.
4.1.2.5.1.2#13	TD 4.005	(Step 11) On reception of a Response from the transmitter, the receiver shall do the following: If (Tx Active = 1b) and (Request Done = 0b), then go to Step 4.
4.1.2.5.1.2#14	TD 4.005	(Step 11) On reception of a Response from the transmitter, the receiver shall do the following: If (Tx Active = 0b) or (Request Done = 1b), repeat Step 9 within tPollTXFFE of receiving the Response.
<b>4.2 Logical Layer State Machine</b>		
<b>4.2.1 Lane Adapter State Machine</b>		
<b>4.2.1.1 Disabled</b>		
<b>4.2.1.1.1 Entry to State</b>		
4.2.1.1.1#1	TD 4.006	An Adapter shall enter this state from Training state or CL0 state when the <i>Lane Disable</i> bit in the Lane Adapter Configuration Capability is set to 1b.
4.2.1.1.1#2	TD 4.006	A Lane Adapter shall set the <i>Plugged</i> bit to 0b upon transitioning to Disabled state.

<b>4.2.1.1.2 Behavior in State</b>		
<b>4.2.1.1.1.3 Exit from State</b>		
4.2.1.1.3#1	NT	An Adapter shall exit this state when the <i>Lane Disable</i> bit in the Lane Adapter Configuration Capability is set to 0b
4.2.1.1.3#2	NT	A disabled Adapter shall stay in the Disabled state for a minimum of tDisabled.
4.2.1.1.3#3	NT	If the <i>Lane Disable</i> bit is set to 0b less than tDisabled after sending the LT_Fall Transaction, the Adapter shall not transition to the CLd state until tDisabled has elapsed.
<b>4.2.1.2 CLd</b>		
<b>4.2.1.2.1 Entry to State</b>		
4.2.1.2.1#1	NT	An Adapter shall enter this state on any of the following events: Router power on.
4.2.1.2.1#2	NT	An Adapter shall enter this state on any of the following events: The USB4 Port is disconnected and <i>Lane Disable</i> bit in the Lane Adapter Configuration Capability is set to 0b.
4.2.1.2.1#3	NT	An Adapter shall enter this state on any of the following events: Router enters Sleep state.
4.2.1.2.1#4	NT	In addition to the events listed above, a Lane Adapter that is not the Upstream Adapter shall enter this state on any of the following events: Adapter exits from the Disabled state.
4.2.1.2.1#5	NT	In addition to the events listed above, a Lane Adapter that is not the Upstream Adapter shall enter this state on any of the following events: Adapter receives an LT_Fall Transaction.
<b>4.2.1.2.2 Behavior in State</b>		
4.2.1.2.2#1	NT	A Lane Adapter that enters this state due to a disconnect shall enter Lane Initialization starting from Phase 1 except for the following cases: Downstream Facing Port Disconnect due to reception of LT_LRoff.
4.2.1.2.2#2	NT	A Lane Adapter that enters this state from the Disabled State performs Lane Initialization after the Lane is enabled. The Lane Adapter shall start Lane Initialization from Phase 4. The USB4 Port shall maintain any state acquired in Phases 1 through 3 of previous Lane Initialization.
4.2.1.2.2#3	NT	A Lane Adapter that enters this state due to the Router entering Sleep state performs Lane Initialization after a Wake event. The Lane Adapter shall start Lane Initialization from Phase 2.



4.2.1.2.2#4	TD 4.033	A Lane Adapter that enters this state due to Link training timeout shall perform Lane Initialization starting from Phase 1
4.2.1.2.2#5	NT	A Lane Adapter (that is not the Upstream Adapter) that enters this state due to reception of an LT_Fall Transaction starts Lane Initialization when it receives a Broadcast RT Transaction. The Lane Adapter shall start Lane Initialization from Phase 4. The USB4 Port shall maintain any state acquired in Phases 1 through 3 of previous Lane Initialization.
4.2.1.2.2#6	NT	The Lane 0 Adapter shall not start Lane Initialization until it receives a Broadcast RT Transaction with the <i>Lane0Enabled</i> bit set to 1b.
4.2.1.2.2#7	NT	The Lane 1 Adapter shall not start Lane Initialization until it receives a Broadcast RT Transaction with the <i>Lane1Enabled</i> bit set to 1b.
<b>4.2.1.2.3 Exit from State</b>		
4.2.1.2.3#1	NT	A Lane Adapter shall exit this state when the Lane's High-Speed transmitter is transmitting (completion of Phase 4 of Lane Initialization) and its receiver is enabled.
4.2.1.2.3#2	TD 4.009	After exiting the CLd state, a Lane Adapter shall transition to the Training.LOCK1 state.
<b>4.2.1.3 Training</b>		
<b>4.2.1.3.1 Entry to State</b>		
4.2.1.3.1#1	NT	A Lane Adapter shall enter this state on any of the following events: After exiting the CLd state.
4.2.1.3.1#2	TD 4.040 TD 4.041	A Lane Adapter shall enter this state on any of the following events: When recovering from a USB4 Link error.
4.2.1.3.1#3	TD 4.010 TD 4.011 TD 4.012 TD 4.013	A Lane Adapter shall enter this state on any of the following events: After exiting the CL2 or CL1 states.
<b>4.2.1.3.2 Behavior in State</b>		
4.2.1.3.2#1	TD 4.009 TD 4.032 TD 4.033	A Lane Adapter shall follow the Training Sub-state machine described in Figure 4-9 with the behavior described in Table 4-19 and the sub-state transitions described in Table 4-20.
4.2.1.3.2#2	TD 4.009	The sub-state transitions shall occur within tTrainingTransition time from receiving the last bit of the relevant Symbols.

4.2.1.3.2#3	NT	In LOCK1 state, a transmitter shall send back-to-back SLOS1.
4.2.1.3.2#4	NT	In LOCK2 state, a transmitter shall send back-to-back SLOS2.
4.2.1.3.2#5	NT	In TS1 state, a transmitter send back-to-back TS1 Ordered Sets.
4.2.1.3.2#6	NT	In TS2 state, a transmitter send back-to-back TS2 Ordered Sets.
<b>4.2.1.3.3 Exit from State</b>		
4.2.1.3.3#1	TD 4.009	A Lane Adapter that transitions from CLd state to Training state shall complete training and transition to the CL0 state within tTrainingAbort1 after entering the Training state.
4.2.1.3.3#2	NT	If the Adapter does not transition to CL0 state within tTrainingAbort1, the Router shall initiate a Disconnect by driving SBTX to a logical low state for tDisconnectTx.
4.2.1.3.3#3	TD 4.040	A Lane Adapter that transitions from a state other than CLd to Training state shall complete training and transition to the CL0 state within tTrainingAbort2 after entering the Training state.
4.2.1.3.3#4	TD 4.033	If the Adapter does not transition to CL0 state within tTrainingAbort2, the Router shall initiate a Disconnect by driving SBTX to a logical low state for tDisconnectTx.
4.2.1.3.3#5	TD 4.006	A Hot Plug Event Packet shall be sent on transition to CL0 state if the Adapter is part of a Downstream Facing Port and it entered Training state from a CLd state.
4.2.1.3.3#6	TD 4.009	A Lane Adapter shall set the Plugged bit to 1b when it transitions from the Training state to the CL0 state.
<b>4.2.1.3.4 SLOS1 and SLOS2</b>		
4.2.1.3.4#1	IOP	When operating in Gen 2 mode with RS-FEC encoding disabled, SLOS shall be encoded using 64b/66b encoding.
4.2.1.3.4#2	IOP	When operating in Gen 2 mode with RS-FEC encoding enabled, SLOS that are not RS-FEC encoded shall be encoded using 128b/132b encoding.
4.2.1.3.4#3	IOP	When operating in Gen 3 mode, SLOS that are not RS-FEC encoded shall be encoded using 128b/132b encoding.
4.2.1.3.4#4	IOP	The SLOS1 and SLOS2 shall not be scrambled, and the scrambler shall not advance upon receive/transmit.
4.2.1.3.4#5	TD 4.009	When transmitting SLOS1 or SLOS2 using 64b/66b encoding, a Router shall transmit all 32 SLOS Symbols in their entirety.
4.2.1.3.4#6	TD 4.009	When using 128b/132b encoding, a Router shall transmit all 16 SLOS Symbols in their entirety.

4.2.1.3.4#7	NT	A Router shall not transmit an incomplete SLOS.
<b>4.2.1.3.5 TS1 and TS2 Ordered Sets</b>		
4.2.1.3.5#1	NT	A TS1 Ordered Set and a TS2 Ordered Set shall have the structure in Table 4-25.
4.2.1.3.5#2	TD 4.036	Bits 63:59 (Rsvd) of a TS1 or TS2 Ordered Set shall be ignored by a receiver.
4.2.1.3.5#3	TD 4.009	Bits 58:56 (Lane Bonding Target) of a TS1 or TS2 Ordered Set shall be set according to the value of the Target Link Width field of the USB4 Adapter Configuration Capability: 000b – Establish two single-Lane Links and 001b – Establish a dual-lane Link. All other values are reserved and shall not be used.
4.2.1.3.5#4	TD 4.009	Bits 55:48 (Lane Number) of a TS1 or TS2 Ordered Set shall be set to match the Lane number: 00h - Lane 0 and 01h - Lane 1. All other values are reserved and shall not be used.
4.2.1.3.5#5	TD 4.009 TD 4.036	Bits 47:32 (Rsvd) of a TS1 or TS2 Ordered Set shall be ignored by a receiver.
4.2.1.3.5#6	BC	Bits 31:29 (Rsvd) of a TS1 or TS2 Ordered Set shall be set to 0 by a transmitter.
4.2.1.3.5#7	TD 4.036	Bits 31:29 (Rsvd) of a TS1 or TS2 Ordered Set shall be ignored by a receiver.
4.2.1.3.5#8	TD 4.009	A Transmitter shall set bits 28:26 (Lane Bonding Target 2) of a TS1 or TS2 Ordered Set to match the Lane Bonding Target field.
4.2.1.3.5#9	TD 4.036	Bits 28:26 (Lane Bonding Target 2) of a TS1 or TS2 Ordered Set shall be ignored by a receiver.
4.2.1.3.5#10	TD 4.036	Bits 25:16 (Rsvd) of a TS1 or TS2 Ordered Set shall be ignored by a receiver.
4.2.1.3.5#11	TD 4.009	Bits 9:0 (SCR) of a TS1 or TS2 Ordered Set shall be set to 00 1111 0010b to indicate that Ordered Set contents are scrambled.
<b>4.2.1.4 CL0</b>		
<b>4.2.1.4.1 Entry to State</b>		
4.2.1.4.1#1	TD 4.005 TD 4.009	A Lane Adapter shall enter this state upon any of the following events: Successful completion of Lane training.
4.2.1.4.1#2	TD 4.009	A Lane Adapter shall enter this state upon any of the following events: Successful completion of Lane Bonding.
4.2.1.4.1#3	TD 4.014 TD 4.015	A Lane Adapter shall enter this state upon any of the following events: Exit from CL0s state

4.2.1.4.2 Behavior in State		
4.2.1.4.3 Exit from State		
4.2.1.4.3#12	NT	A Lane Adapter shall exit this state after one of the following occurs: Adapter Disable.
4.2.1.4.3#13	NT	A Lane Adapter that exits this state due to an Adapter disable shall transition to either the Disabled state or the CLd state as defined in Section 4.4.6.
4.2.1.4.3#14	NT	A Lane Adapter shall exit this state after one of the following occurs: Adapter disconnect. An Adapter that exits this state due to a disconnect event shall transition to the CLd state.
4.2.1.4.3#15	NT	A Lane Adapter shall exit this state after one of the following occurs: Reception of an LT_Fall Transaction. The Adapter shall transition to the CLd state.
4.2.1.4.3#16	TD 4.040 TD 4.041	A Lane Adapter shall exit this state after one of the following occurs: Transition to Training state when: An error event occurs that transitions the Lane Adapter to the Training.LOCK1 state.
4.2.1.4.3#17	TD 4.032 TD 4.033	A Lane Adapter shall exit this state after one of the following occurs: Transition to Training state when: Reception of any 2 SLOS Symbols in a row transitions the Lane Adapter either to the Training.LOCK1 sub-state or to the Training.LOCK2 sub-state.
4.2.1.4.3#18	NT	A Lane Adapter shall exit this state after one of the following occurs: Transition to CL0s, CL1, or CL2 states.
4.2.1.4.3#19	TD 4.009 TD 4.010 TD 4.011 TD 4.014 TD 4.015	A Lane Adapter shall exit this state after one of the following occurs: Transition to Lane Bonding state when either: The <i>Lane Bonding</i> bit in the USB4 Adapter Configuration Capability Register of either Adapter in the USB4 Port is set to 1b.
4.2.1.4.3#20	TD 4.010	A Lane Adapter shall exit this state after one of the following occurs: Transition to Lane Bonding state when either: 3 TS1 Ordered Sets are received in a row.
4.2.1.4.3#21	NT	A Lane Adapter shall not exit this state to enter Lane Bonding state while it is sending a Transport Layer Packet.
4.2.1.4.3#22	NT	The Adapter shall complete sending the packet before entering Lane Bonding state.

<b>4.2.1.5 Lane Bonding</b>		
<b>4.2.1.5.1 Entry to State</b>		
4.2.1.5.1#1	TD 4.009	A Lane Adapter shall enter this state from CL0 state on any of the following events: The Lane Bonding bit in the Lane Adapter Capability Register of either Adapter in the USB4 Port is set to 1b.
4.2.1.5.1#2	TD 4.009	An Adapter shall enter this state from CL0 state on any of the following events: Three TS1 Ordered Sets are received in a row.
<b>4.2.1.5.2 Behavior in State</b>		
4.2.1.5.2#1	TD 4.009 TD 4.034	A Lane Adapter shall follow the Lane Bonding sub-state machine described in Figure 4-10 with the behavior described in Table 4-26 and the state transitions described in Table 4-27.
4.2.1.5.2#2	NT	In TS1 state, transmitter shall send back-to-back TS1 Ordered Sets.
4.2.1.5.2#3	NT	In TS2 state, transmitter shall send back-to-back TS2 Ordered Sets.
<b>4.2.1.5.3 Exit from State</b>		
4.2.1.5.3#1	TD 4.009	A Lane Adapter shall exit this state as defined in Table 4-27.
4.2.1.5.3#2	TD 4.009	A Lane Adapter that exits this state due to successful completion shall transition to the CL0 state.
4.2.1.5.3#3	TD 4.009	A Lane Adapter that transitions to CL0 state shall continue sending TS2 Ordered Sets until the other Adapter enters CL0 state.
4.2.1.5.3#4	NT	A Lane Adapter that exits this state due to unsuccessful completion (i.e. Transitions 2, 4, and 5 in Table 4-27) shall transition to the Training.LOCK2 sub-state
<b>4.2.1.6 Low Power (CL0s, CL1, CL2)</b>		
4.2.1.6#1	NT	When a Lane Adapter supports CLx states, it shall enter or reject a CLx state as described in Section 4.2.1.6.2.
4.2.1.6#2	NT	When a Lane Adapter does not support CLx states, it shall reject entry to CLx state as described in Section 4.2.1.6.2.
<b>4.2.1.6.1 Ordered Sets</b>		
4.2.1.6.1#1	NT	Bits 9:0 (SCR) in a CL2_REQ Ordered Set payload shall be set to 00 1111 0010b to indicate that the Ordered Set contents are scrambled.
4.2.1.6.1#2	NT	Bits 9:0 (SCR) in a CL1_REQ Ordered Set payload shall be set to 00 1111 0010b to indicate that the Ordered Set contents are scrambled.

4.2.1.6.1#3	TD 4.010 TD 4.011	Bits 9:0 (SCR) in a CL2_ACK Ordered Set payload shall be set to 00 1111 0010b to indicate that the Ordered Set contents are scrambled.
4.2.1.6.1#4	TD 4.012 TD 4.013	Bits 9:0 (SCR) in a CL1_ACK Ordered Set payload shall be set to 00 1111 0010b to indicate that the Ordered Set contents are scrambled.
4.2.1.6.1#5	TD 4.014 TD 4.015	Bits 9:0 (SCR) in a CL0s_ACK Ordered Set payload shall be set to 00 1111 0010b to indicate that the Ordered Set contents are scrambled.
4.2.1.6.1#6	TD 4.010 TD 4.011 TD 4.012 TD 4.013	Bits 9:0 (SCR) in a CL_NACK Ordered Set payload shall be set to 00 1111 0010b to indicate that the Ordered Set contents are scrambled.
4.2.1.6.1#7	NT	Bits 9:0 (SCR) in a CL_OFF Ordered Set payload shall be set to 00 1111 0010b to indicate that the Ordered Set contents are scrambled.
<b>4.2.1.6.1.1 CL_WAKE1.X Ordered Sets</b>		
4.2.1.6.1.1#1	NT	A CL_WAKE1.X Ordered Set shall not be scrambled, and the scrambler shall not advance upon receive/transmit.
4.2.1.6.1.1#2	NT	Unless otherwise mentioned, a CL_WAKE1.X Ordered Set shall be transmitted in its entirety.
<b>4.2.1.6.1.2 CL_WAKE2.X Ordered Sets</b>		
4.2.1.6.1.2#1	NT	When operating in Gen 2 mode with RS-FEC encoding disabled, a CL_WAKE2.X Ordered Set has the structure of an SLOS2 with 64/66b encoding and the following modifications: Bits [63:56] of an even numbered Symbol payload shall be CXh, where "X" is the hexadecimal index from the last CL_WAKE1.X Ordered Set received.
4.2.1.6.1.2#2	NT	When operating in Gen 2 mode with RS-FEC encoding disabled, a CL_WAKE2.X Ordered Set has the structure of an SLOS2 with 64/66b encoding and the following modifications: Bits [63:56] of an odd numbered Symbol payload shall be the logical inverse of CXh, where "X" is the hexadecimal index from the last CL_WAKE1.X Ordered Set received.
4.2.1.6.1.2#3	NT	When operating in Gen 2 mode and RS-FEC encoding is enabled, a CL_WAKE2.X Ordered Set has the structure of an SLOS2 with 128b/132b Encoding and the following modifications: Bits [127:120] of an even numbered Symbol payload shall be CXh, where "X" is the hexadecimal index from the last CL_WAKE1.X Ordered Set received.
4.2.1.6.1.2#4	NT	When operating in Gen 2 mode and RS-FEC encoding is enabled, a CL_WAKE2.X Ordered Set has the structure of an SLOS2 with 128b/132b Encoding and the following modifications: Bits [63:56] of an even numbered Symbol payload shall be CXh, where "X" is the hexadecimal index from the last CL_WAKE1.X Ordered Set received.

4.2.1.6.1.2#5	NT	When operating in Gen 2 mode and RS-FEC encoding is enabled, a CL_WAKE2.X Ordered Set has the structure of an SLOS2 with 128b/132b Encoding and the following modifications: Bits [127:120] of an odd numbered Symbol payload shall be the logical inverse of CXh, where “X” is the hexadecimal index from the last CL_WAKE1.X Ordered Set received.
4.2.1.6.1.2#6	NT	When operating in Gen 2 mode and RS-FEC encoding is enabled, a CL_WAKE2.X Ordered Set has the structure of an SLOS2 with 128b/132b Encoding and the following modifications: Bits [63:56] of an odd numbered Symbol payload shall be the logical inverse of CXh, where “X” is the hexadecimal index from the last CL_WAKE1.X Ordered Set received.
4.2.1.6.1.2#7	NT	When operating in Gen 3 mode, a CL_WAKE2.X Ordered Set has the structure of an SLOS2 with 128b/132b Encoding and the following modifications: Bits [127:120] of an even numbered Symbol payload shall be CXh, where “X” is the hexadecimal index from the last CL_WAKE1.X Ordered Set received.
4.2.1.6.1.2#8	NT	When operating in Gen 3 mode, a CL_WAKE2.X Ordered Set has the structure of an SLOS2 with 128b/132b Encoding and the following modifications: Bits [127:120] of an odd numbered Symbol payload shall be the logical inverse of CXh, where “X” is the hexadecimal index from the last CL_WAKE1.X Ordered Set received.
4.2.1.6.1.2#9	TD 4.011 TD 4.013	A CL_WAKE2.X Ordered Set shall not be scrambled, and the scrambler shall not advance upon receive/transmit.
4.2.1.6.1.2#10	TD 4.011 TD 4.013	Unless otherwise mentioned, a CL_WAKE2.X Ordered Set shall be transmitted in its entirety.
<b>4.2.1.6.2 Entry to State</b>		
4.2.1.6.2#41	TD 4.010 TD 4.011 TD 4.012 TD 4.013	(Requesting Port) The request Ordered Set shall be sent back-to-back until a response Ordered Set is received from the Link Partner.
4.2.1.6.2#42	NT	(Requesting Port) An Adapter shall send CL2_REQ Ordered Sets when its USB4 Port does not assert any objections to enter CL2 state.
4.2.1.6.2#43	NT	(Requesting Port) An Adapter shall send CL1_REQ Ordered Sets when its USB4 Port asserts an objection to enter CL2 state but does not assert any objections to enter CL1 state.
4.2.1.6.2#44	NT	(Requesting Port) If a Lane Adapter receives a CL1_REQ Ordered Set or a CL2_REQ Ordered Set from its Link Partner, it shall not request entry to a Low Power state until after transitioning back to CL0.

4.2.1.6.2#45	NT	(Requesting Port) If the Requesting Port asserts an objection after the Lane Adapter has sent a request Ordered Set, the Lane Adapter shall ignore the objection until the Lane Adapter is either in a CLx state or receives a CL_NACK Ordered Set.
4.2.1.6.2#46	NT	(Responding Port) A Lane Adapter shall reject a request to enter a Low Power state when all of the following are true: The Adapter has already sent a request to enter the same low power state; and The <i>PM Secondary</i> bit in the Lane 0 Adapter and/or the Lane 1 Adapter of the Responding Port is set to 0b.
4.2.1.6.2#47	TD 4.010 TD 4.011 TD 4.012 TD 4.013	The Lane Adapter shall send CL_NACK Ordered Sets for as long as it receives the request Ordered Set from the Link Partner.
4.2.1.6.2#48	NT	A Lane Adapter that receives a CL1_REQ Ordered Set after it has sent a CL2_REQ Ordered Set, shall accept the request by responding with CL1_ACK Ordered Sets. The Adapter shall stop sending CL2_REQ Ordered Sets.
4.2.1.6.2#49	NT	A Lane Adapter that receives a CL2_REQ Ordered Set after it has sent a CL1_REQ Ordered Set, shall not respond to the request and shall continue sending CL1_REQ Ordered Sets.
4.2.1.6.2#50	TD 4.010 TD 4.011	Else, if the Responding Port does not assert an objection to enter CL2 state, it shall respond to CL2_REQ Ordered Sets with a CL2_ACK Ordered Set. The CL2_ACK Ordered Set shall be sent 375 times.
4.2.1.6.2#51	TD 4.012 TD 4.013	Else, if the Responding Port does not assert an objection to enter CL1 state, it shall respond to CL2_REQ or CL1_REQ Ordered Sets with a CL1_ACK Ordered Set. The CL1_ACK Ordered Set shall be sent 375 times.
4.2.1.6.2#52	TD 4.014 TD 4.015	Else, if the <i>CL0s Enable</i> bit is set to 1b in the Lane 0 Adapter of the Responding Port, a Lane Adapter shall respond to a request to enter a Low Power state with a CL0s_ACK Ordered Set. The CL0s_ACK Ordered Set shall be sent 16 times.
4.2.1.6.2#53	TD 4.010 TD 4.011 TD 4.012 TD 4.013	Else, a Lane Adapter shall respond to a request to enter a Low Power state with CL_NACK Ordered Sets. The CL_NACK Ordered Sets shall be sent 16 times.
4.2.1.6.2#54	TD 4.010 TD 4.011 TD 4.012 TD 4.013	The Adapter shall resume regular CL0 operation in the transmit direction once it stops sending the CL_NACK Ordered Sets.



4.2.1.6.2#55	NT	If the Responding Port asserts an objection after the Lane Adapter has sent a CLx_ACK response Ordered Set, but before the transition to CLx state is complete, the Lane Adapter shall ignore the objection until it transitions to the CLx state.
4.2.1.6.2#56	NT	A Lane Adapter shall stop sending a request to enter a Low Power state when it receives a response Ordered Set from the Link Partner.
4.2.1.6.2#57	TD 4.010 TD 4.011 TD 4.012 TD 4.013	(Requesting Port) If the response is a CL2_ACK, a CL1_ACK, or a CL0s_ACK Ordered Set, the Lane Adapter shall send 375 CL_OFF Ordered Sets. The CL_OFF Ordered sets shall be sent back-to-back.
4.2.1.6.2#58	TD 4.010 TD 4.011 TD 4.012 TD 4.013	(Requesting Port) The first CL_OFF Ordered Set shall be sent within tCLxResponse after detection of the response.
4.2.1.6.2#59	TD 4.010 TD 4.011 TD 4.012 TD 4.013	(Requesting Port) If the response is a CL2_ACK or a CL1_ACK Ordered Set, the Adapter shall also shut down its receiver.
4.2.1.6.2#60	TD 4.010 TD 4.011 TD 4.012 TD 4.013	(Requesting Port) If the response is a CL_NACK Ordered Set, the Adapter shall not send another CL2_REQ Ordered Set or CL1_REQ Ordered Set for tCLxRetry after receiving the CL_NACK Ordered Set.
4.2.1.6.2#61	TD 4.010 TD 4.011 TD 4.012 TD 4.013	(Requesting Port) If the response is a CL_NACK Ordered Set, all Lane Adapters in the Requesting Port shall resume regular CL0 operation.
4.2.1.6.2#62	NT	If the Requesting Port detects Link errors in the direction of the Link Partner before receiving a response Ordered Set from the Link Partner, it shall: Stop sending the request to enter a Low Power state.
4.2.1.6.2#63	NT	If the Requesting Port detects Link errors in the direction of the Link Partner before receiving a response Ordered Set from the Link Partner, it shall: Transition its Lane Adapters to the Training.LOCK1 sub-state and send the first SLOS within tCLxResponse of detecting the Link error.

4.2.1.6.2#64	TD 4.010 TD 4.011 TD 4.012 TD 4.013	In the Requesting Port, a Lane Adapter shall do the following after sending 375 CL_OFF Ordered Sets: 1. Shut down its transmitter within tTxOff time.
4.2.1.6.2#65	TD 4.010 TD 4.011	In the Requesting Port, a Lane Adapter shall do the following after sending 375 CL_OFF Ordered Sets: 2. Transition state as follows: If the response from the Link Partner was CL2_ACK, transition to CL2 state.
4.2.1.6.2#66	TD 4.012 TD 4.013	In the Requesting Port, a Lane Adapter shall do the following after sending 375 CL_OFF Ordered Sets: 2. Transition state as follows: If the response from the Link Partner was CL1_ACK, transition to CL1 state.
4.2.1.6.2#67	NT	In the Requesting Port, a Lane Adapter shall do the following after sending 375 CL_OFF Ordered Sets: 2. Transition state as follows: If the response from the Link Partner was CL0s_ACK, transition to CL0s state.
4.2.1.6.2#68	NT	In the Requesting Port, a Lane Adapter shall do the following after sending 375 CL_OFF Ordered Sets: 3. Enable exit from CLx state as follows: If the response from the Link Partner was CL2_ACK or CL1_ACK, wait tEnterLFPS1 time after the state transition in Step 2), then enable transmission and detection of Low Frequency Periodic Signaling (LFPS).
4.2.1.6.2#69	NT	In the Requesting Port, a Lane Adapter shall do the following after sending 375 CL_OFF Ordered Sets: 3. Enable exit from CLx state as follows: If the response from the Link Partner was CL0s_ACK, wait tEnterLFPS4 time after the state transition in Step 2), then enable transmission of Low Frequency Periodic Signaling (LFPS).
4.2.1.6.2#70	TD 4.010 TD 4.011 TD 4.012 TD 4.013 TD 4.014 TD 4.015	In the Responding Port, a Lane Adapter shall shut down its receiver after receiving a CL_OFF Ordered Set. If the Adapter sent CL0s_ACK Ordered Sets, it shall also transition to the CL0s state.
4.2.1.6.2#71	NT	In the Responding Port, The Adapter shall then enable exit from the Low Power state as follows: If the Adapter sent CL2_ACK or CL1_ACK, wait tEnterLFPS2 time after shutting down the receiver, then enable transmission and detection of Low Frequency Periodic Signaling (LFPS).
4.2.1.6.2#72	NT	In the Responding Port, The Adapter shall then enable exit from the Low Power state as follows: If the Adapter sent CL0s_ACK, wait tEnterLFPS5, then enable detection of Low Frequency Periodic Signaling (LFPS).

4.2.1.6.2#73	TD 4.010 TD 4.011	In the Responding Port, a Lane Adapter shall do the following after the equivalent of 375 Symbol Times has passed since sending the first response Ordered Set: If the Adapter sent CL2_ACK Ordered Sets, it shall shut down its transmitter and shall shut down its receiver if it has not done so already. It shall then transition to the CL2 state
4.2.1.6.2#74	TD 4.012 TD 4.013	In the Responding Port, a Lane Adapter shall do the following after the equivalent of 375 Symbol Times has passed since sending the first response Ordered Set: If the Adapter sent CL1_ACK Ordered Sets, it shall shut down its transmitter and shall shut down its receiver if it has not done so already. It shall then transition to the CL1 state.
4.2.1.6.2#75	TD 4.015	In the Responding Port, a Lane Adapter shall do the following after the equivalent of 375 Symbol Times has passed since sending the first response Ordered Set: If the Adapter sent CL0s_ACK Ordered Sets, it shall shut down its receiver if it has not done so already. It shall then transition to the CL0s state.
4.2.1.6.2#76	NT	In the Responding Port, a Lane Adapter shall do the following after the equivalent of 375 Symbol Times has passed since sending the first response Ordered Set: Enable exit from CLx state as follows: If the Adapter sent CL2_ACK or CL1_ACK Ordered Sets, wait tEnterLFPS3 time, then enable transmission and detection of Low Frequency Periodic Signaling (LFPS).
4.2.1.6.2#77	NT	In the Responding Port, a Lane Adapter shall do the following after the equivalent of 375 Symbol Times has passed since sending the first response Ordered Set: Enable exit from CLx state as follows: If the Adapter sent CL0s_ACK Ordered Sets, wait 240 Symbol Times + 100ns, then enable detection of Low Frequency Periodic Signaling (LFPS).
4.2.1.6.2#78	TD 4.037	A Lane Adapter may transition to Training.LOCK1 sub-state as a result of Logical Layer errors during the entry to Low Power state with the following exceptions: After sending the first CL2_ACK, CL1_ACK, or CL0s_ACK Ordered Set, a Lane Adapter shall not enter Training state as a result of Logical Layer errors in its receivers.
4.2.1.6.2#79	NT	A Lane Adapter may transition to Training.LOCK1 sub-state as a result of Logical Layer errors during the entry to Low Power state with the following exceptions: A Lane Adapter that is sending CL_OFF Ordered Sets shall complete the transition to CL2, CL1, or CL0s state.
<b>4.2.1.6.3 Objections</b>		
4.2.1.6.3#31	TD 4.010 TD 4.011	A USB4 Port shall assert an objection to enter CL2 state if: The <i>CL2 Support</i> bit in the Lane 0 Adapter is 0.
4.2.1.6.3#32	NT	A USB4 Port shall assert an objection to enter CL2 state if: The <i>CL2 Enable</i> bit in the Lane 0 Adapter is 0b.
4.2.1.6.3#33	NT	A USB4 Port shall assert an objection to enter CL2 state if: There is a Transport Layer Packet to be sent over the USB4 Port.

4.2.1.6.3#34	NT	A USB4 Port shall assert an objection to enter CL2 state if: The Lane 0 Adapter is referenced in an <i>Egress Adapter</i> field of a PCIe Adapter's Routing Table and the PCIe Adapter is not in PCIe L1 state.
4.2.1.6.3#35	NT	A USB4 Port shall assert an objection to enter CL2 state if: The Lane 0 Adapter is referenced in an <i>Egress Adapter</i> field of the Upstream PCIe Adapter's Routing Table, and either the No-Snoop Latency value or the Snoop Latency value in the last LTR Message transmitted upstream is smaller than the sum of the CL2 entry and exit latency.
4.2.1.6.3#36	NT	A USB4 Port shall assert an objection to enter CL2 state if: The Lane 0 Adapter is referenced in an <i>Egress Adapter</i> field of a Downstream PCIe Adapter's Routing Table, and either the No-Snoop Latency value or the Snoop Latency value in the last LTR Message received by the Downstream PCIe Adapter is smaller than the sum of the CL2 entry and exit latency.
4.2.1.6.3#37	NT	A USB4 Port shall assert an objection to enter CL2 state if: The Lane 0 Adapter is referenced in an <i>Egress Adapter</i> field of a DP IN Adapter's Routing Table.
4.2.1.6.3#38	NT	A USB4 Port shall assert an objection to enter CL2 state if: The Lane 0 Adapter is referenced in an <i>Egress Adapter</i> field of a DP OUT Adapter's Routing Table and a Packet is issued from the DP OUT Adapter.
4.2.1.6.3#39	NT	A USB4 Port shall assert an objection to enter CL2 state if: The Lane 0 Adapter is referenced in an <i>Egress Adapter</i> field of a USB3 Adapter's Routing Table and the USB3 link between the USB3 Adapter and the internal USB3 device is not in U2 or U3 state.
4.2.1.6.3#40	NT	A USB4 Port shall assert an objection to enter CL2 state if: The Lane 0 Adapter is referenced in an <i>Egress Adapter</i> field of a USB3 Adapter's Routing Table, the USB3 link between the USB3 Adapter and the internal USB3 device is in U2 state, and CL2 entry is disabled in U2 state.
4.2.1.6.3#41	NT	A USB4 Port shall assert an objection to enter CL2 state if: The Lane 0 Adapter is referenced in an <i>Egress Adapter</i> field of a USB3 Adapter's Routing Table, the USB3 link between the USB3 Adapter and the internal USB3 device is in U3 state, and CL2 entry is disabled in U3 state.
4.2.1.6.3#42	NT	A USB4 Port shall assert an objection to enter CL2 state if: Entry to CL2 state would delay a pending Time Sync handshake. This objection shall be asserted until the Time Sync handshake is complete.
4.2.1.6.3#43	NT	(Host Routers Only) A USB4 Port shall assert an objection to enter CL2 state if: The Lane 0 Adapter is referenced in an <i>Egress Adapter</i> field of a Host Interface Adapter's Routing Table, whose Path corresponds to a Transmit Descriptor Ring that disables CL2 entry.
4.2.1.6.3#44	NT	(Host Routers Only) A USB4 Port shall assert an objection to enter CL2 state if: The Lane 0 Adapter is referenced in an <i>Egress Adapter</i> field of a Host Interface Adapter's Routing Table and the Host Interface has a Packet to send over the Adapter.

4.2.1.6.3#45	NT	(Device Routers Only) One of its Ports is in the process of CL0s, CL1 or CL2 exit flow.
4.2.1.6.3#46	TD 4.012 TD 4.013	A USB4 Port shall assert an objection to enter CL1 state if: The <i>CL1 Support</i> bit in the Lane 0 Adapter is 0b.
4.2.1.6.3#47	NT	A USB4 Port shall assert an objection to enter CL1 state if: The <i>CL1 Enable</i> bit in the Lane 0 Adapter is 0b.
4.2.1.6.3#48	NT	A USB4 Port shall assert an objection to enter CL1 state if: There is a Transport Layer Packet to be sent over the USB4 Port.
4.2.1.6.3#49	NT	A USB4 Port shall assert an objection to enter CL1 state if: The Lane 0 Adapter is referenced in an <i>Egress Adapter</i> field of a PCIe Adapter's Routing Table and the PCIe Adapter is not in PCIe L1 state.
4.2.1.6.3#50	NT	A USB4 Port shall assert an objection to enter CL1 state if: The Lane 0 Adapter is referenced in an <i>Egress Adapter</i> field of the Upstream PCIe Adapter's Routing Table, and either the No-Snoop Latency value or the Snoop Latency value in the last LTR Message transmitted upstream is smaller than the sum of the CL1 entry and exit latency.
4.2.1.6.3#51	NT	A USB4 Port shall assert an objection to enter CL1 state if: The Lane 0 Adapter is referenced in an <i>Egress Adapter</i> field of a Downstream PCIe Adapter's Routing Table, and either the No-Snoop Latency value or the Snoop Latency value in the last LTR Message received by the Downstream PCIe Adapter is smaller than the sum of the CL1 entry and exit latency.
4.2.1.6.3#52	NT	A USB4 Port shall assert an objection to enter CL1 state if: The Lane 0 Adapter is referenced in an <i>Egress Adapter</i> field of a DP IN Adapter's Routing Table.
4.2.1.6.3#53	NT	A USB4 Port shall assert an objection to enter CL1 state if: The Lane 0 Adapter is referenced in an <i>Egress Adapter</i> field of a DP OUT Adapter's Routing Table and a Packet is issued from the DP OUT Adapter.
4.2.1.6.3#54	NT	A USB4 Port shall assert an objection to enter CL1 state if: The Lane 0 Adapter is referenced in an <i>Egress Adapter</i> field of a USB3 Adapter's Routing Table and the USB3 link between the USB3 Adapter and the internal USB3 device is not in U2 or U3 state.
4.2.1.6.3#55	NT	A USB4 Port shall assert an objection to enter CL1 state if: The Lane 0 Adapter is referenced in an <i>Egress Adapter</i> field of a USB3 Adapter's Routing Table, the USB3 link between the USB3 Adapter and the internal USB3 device is in U3 state, and CL1 entry is disabled in USB U3 state.
4.2.1.6.3#56	NT	A USB4 Port shall assert an objection to enter CL1 state if: The Lane 0 Adapter is referenced in an <i>Egress Adapter</i> field of a USB3 Adapter's Routing Table, the USB3 Adapter is in USB U3 state, and CL1 entry is disabled in USB U3 state.

4.2.1.6.3#57	NT	A USB4 Port shall assert an objection to enter CL1 state if: Entry to CL1 state would delay a pending Time Sync handshake.
4.2.1.6.3#58	NT	(Host Routers Only) A USB4 Port shall assert an objection to enter CL1 state if: The Lane 0 Adapter is referenced in an <i>Egress Adapter</i> field of a Host Interface Adapter's Routing Table, whose Path corresponds to a Transmit Descriptor Ring that disables CL1 entry.
4.2.1.6.3#59	NT	(Host Routers Only) A USB4 Port shall assert an objection to enter CL1 state if: The Lane 0 Adapter is referenced in an <i>Egress Adapter</i> field of a Host Interface Adapter's Routing Table and the Host Interface has a Packet to send over the Adapter.
4.2.1.6.3#60	NT	(Device Routers Only) One of its Ports is in the process of CL0s, CL1 or CL2 exit flow.
<b>4.2.1.6.4 Behavior in State</b>		
4.2.1.6.4#1	TD 4.010 TD 4.011	While in CL2 state, the transmitter shall be in electrical idle. Lane common mode voltages shall be maintained.
4.2.1.6.4#2	TD 4.012 TD 4.013	While in CL1 state, the transmitter shall be in electrical idle. Lane common mode voltages shall be maintained.
4.2.1.6.4#3	TD 4.014 TD 4.015	While in CL0s state, the transmitter at the requesting USB4 Port shall be in electrical idle. Lane common mode voltages shall be maintained.
4.2.1.6.4#4	TD 4.010 TD 4.011 TD 4.012 TD 4.013 TD 4.014 TD 4.015	Receiver termination shall be maintained in CL0s CL1, and CL2 states.
<b>4.2.1.6.5 Exit from State</b>		
4.2.1.6.5#1	TD 4.016	A Lane Adapter shall initiate transition out of CL2, CL1, or CL0s state when: An objection is set in the USB4 Port that would have prevented the Adapter from entering the low power state.
4.2.1.6.5#2	NT	A Lane Adapter shall initiate transition out of CL2, CL1, or CL0s state when: The Adapter is in CL0s state and a CL2_REQ Ordered Set or a CL1_REQ Ordered Set is received from the Link Partner.
4.2.1.6.5#3	NT	A Lane Adapter shall initiate transition out of CL2, CL1, or CL0s state when: The Adapter is in CL0s state and it detects Link errors that cause the Adapter to transition to Training state.

4.2.1.6.5#4	NT	A Lane Adapter shall initiate transition out of CL2, CL1, or CL0s state when: The Adapter is in a CL1 state or a CL2 state and it is referenced in an <i>Egress Adapter</i> field of a Lane Adapter's Routing Table and the other Adapter's receiver is exiting from CL0s, CL1, or CL2 states.
4.2.1.6.5#5	NT	A Lane Adapter shall initiate transition out of CL2, CL1, or CL0s state when: The Adapter is in CL0s state and it is referenced in an <i>Egress Adapter</i> field of a Lane Adapter's Routing Table and the other Adapter's receiver is exiting from CL0s, CL1, or CL2 states.
<b>4.2.1.6.5.1 Exit Flow from CL0s State</b>		
4.2.1.6.5.1#1	TD 4.014 TD 4.015 TD 4.016	The USB4 Port initiating exit from CL0s state shall: 1. Send a Low Frequency Periodic Signaling (LFPS) burst on all Lanes for the duration of at least 16 LFPS cycles.
4.2.1.6.5.1#2	TD 4.016	The USB4 Port initiating exit from CL0s state shall: 2. Return to Electrical Idle for tPreData.
4.2.1.6.5.1#3	TD 4.016	The USB4 Port initiating exit from CL0s state shall: 3. Start transmitting SLOS1 on each Lane of the USB4 Port. Any received CL_WAKE Ordered Sets shall be ignored.
4.2.1.6.5.1#4	TD 4.016	The USB4 Port initiating exit from CL0s state shall: 4. On detection of 2 back-to-back TS2 Ordered Sets, stop sending SLOS1 and send at least 16 TS2 Ordered Sets.
4.2.1.6.5.1#5	TBD	The first TS2 Ordered Set shall be sent within tTrainingTransition after detection of the second TS2 Ordered Set.
4.2.1.6.5.1#6	NT	Before transmitting the first TS2 Ordered Sets: The scrambler shall load a new seed; Activate RS-FEC; Enable SSC if SSC is disabled.
4.2.1.6.5.1#7	TBD	If the receiver did not detect 2 back-to-back TS2 Ordered Sets within tTrainingAbort2 time after the transmitter started sending SLOS1 it shall initiate a Disconnect by driving SBTX to a logical low state for tDisconnectTx.
4.2.1.6.5.1#8	TD 4.016	The USB4 Port initiating exit from CL0s state shall: 5. Transition to CL0 state.
4.2.1.6.5.1#9	TD 4.016	If the USB4 Port operated as a Dual-Lane Link prior to entry to CL0s state, the USB4 Port shall resume operation as a Dual-Lane Link independent of the setting of the TS2 Ordered Sets. A de-skew Ordered Set shall be sent. The scrambler shall load a new seed.
4.2.1.6.5.1#10	NT	If the Router initiated exit from CL0s state due to receiving CL1_REQ or CL2_REQ Ordered Sets, then the Router shall respond to the request Ordered Sets. The Router shall not send any Transport Layer Packets before completing the CLx entry flow.

4.2.1.6.5.1#11	TD 4.014 TD 4.015	Upon detecting 2 LFPS cycles, a Lane Adapter in CL0s state shall: 1. Enable the receiver to start bit and symbol synchronization not earlier than tCLxIdleRx after the last LFPS cycle received. An Adapter shall complete Symbol lock within tWarmUpCL0s time from the reception of the first LFPS cycle.
4.2.1.6.5.1#12	TD 4.014 TD 4.015	Upon detecting 2 LFPS cycles, a Lane Adapter in CL0s state shall: 2. On reception of 3 back-to-back CL_WAKE1.X Ordered Set Symbols by the Lane 0 Adapter, transmit at least 8 CL_WAKE2.X Ordered Set Symbols on each enabled Lane of the USB4 Port.
4.2.1.6.5.1#13	TD 4.038	If 3 back-to-back CL_WAKE1.(X+1) Ordered Set Symbols or 3 back-to-back SLOS Symbols are not received within tCL0sSwitch time after receiving a CL_WAKE1.X Ordered Set Symbol, then the Adapter shall transition to the Training.LOCK1 sub-state.
4.2.1.6.5.1#14	NT	If the Router initiated exit from CL0s state by sending CL1_REQ or CL2_REQ Ordered Sets, then the Router shall continue sending the Ordered Sets instead of sending Transport Layer Packets. The Router shall not send any Transport Layer Packets after sending the first CL1_REQ or a CL2_REQ Ordered Set.
4.2.1.6.5.1#15	TD 4.014 TD 4.015	Upon detecting 2 LFPS cycles, a Lane Adapter in CL0s state shall: 3. On detection of 3 back-to-back SLOS Symbols by all enabled Adapters of the USB4 Port, transmit 16 TS2 Ordered Sets in each enabled Lane of the USB4 Port
4.2.1.6.5.1#16	TD 4.014 TD 4.015	Upon detecting 2 LFPS cycles, a Lane Adapter in CL0s state shall: 4. On detection of 2 back-to-back TS2 Ordered Sets, transition to CL0 state: If the Router initiated exit from CL0s state by sending CL1_REQ or CL2_REQ Ordered Sets, then the Router shall continue to send the Ordered Sets. The Router shall not send any Transport Layer Packets before completing the CLx entry flow.
4.2.1.6.5.1#17	TD 4.038	Upon detecting 2 LFPS cycles, a Lane Adapter in CL0s state shall: 4. On detection of 2 back-to-back TS2 Ordered Sets, transition to CL0 state: If the Adapter does not detect 2 back-to-back TS2 Ordered Sets in tTS2Timeout from transmitting TS2 Ordered Sets, the Lane Adapters in the Port shall enter the Training state.
4.2.1.6.5.1#18	TBD	In order to limit the CL0s exit time to 245μs, a Router shall comply with the following equation: $tWarmUpCL0s = 6 \times tWakeResponse + tTrainingTransition < 80 \mu s$ .
4.2.1.6.5.1#19	NT	If the Link is operating at Gen 2 speed, the Adapter may transmit a partial CL_WAKE2.X Ordered Set in order to send the required number of CL_WAKE2.X Ordered Set Symbols. Otherwise, the Wake Ordered Set shall be transmitted in its entirety.



<b>4.2.1.6.5.2 Exit Flow from CL1 or CL2 State (No Re-timers on the Link)</b>		
4.2.1.6.5.2#1	TD 4.016 TD 4.010 TD 4.012	The USB4 Port initiating exit from CL1 or CL2 state shall: 1. Send a Low Frequency Periodic Signaling (LFPS) burst on each Lane until the receiver detects LFPS.
4.2.1.6.5.2#2	TBD	If the receiver did not detect LFPS after tTrainingAbort2 time the Router shall initiate a Disconnect by driving SBTX to a logical low state for tDisconnectTx.
4.2.1.6.5.2#3	TD 4.016 TD 4.010 TD 4.012	The USB4 Port initiating exit from CL1 or CL2 state shall: 2. Return to Electrical Idle for tPreData.
4.2.1.6.5.2#4	TD 4.016 TD 4.010 TD 4.012	The USB4 Port initiating exit from CL1 or CL2 state shall: 3. Start transmitting SLOS1 on the Lane.
4.2.1.6.5.2#5	TD 4.016 TD 4.010 TD 4.012	The USB4 Port initiating exit from CL1 or CL2 state shall: 4. Enable the receiver to start bit and symbol synchronization not earlier than tCLxIdleRx after the last LFPS cycle received. A Lane Adapter shall complete Symbol lock within tRxLock time.
4.2.1.6.5.2#6	TD 4.016 TD 4.010 TD 4.012	The USB4 Port initiating exit from CL1 or CL2 state shall: 5. Transition the Lane Adapter to Training.LOCK1 sub-state.
4.2.1.6.5.2#7	NT	On transition to the TS1 sub-state, the USB4 Port shall enable SSC if SSC is disabled.
4.2.1.6.5.2#8	TD 4.010 TD 4.012	Upon detecting 2 LFPS cycles, a Lane Adapter in CL1 or CL2 state shall: 1. Send a Low Frequency Periodic Signaling (LFPS) burst on the Lane for the duration of at least 3 LFPS cycles and for no more than tLFPSDuration. If the Lane Adapter is in CL1 state, the first LFPS shall be sent within tWarmUpCL1 after receiving the first LFPS cycle. If the Lane Adapter is in CL2 state, the first LFPS shall be sent within tWarmUpCL2 after receiving the first LFPS cycle.
4.2.1.6.5.2#9	TD 4.010 TD 4.012	Upon detecting 2 LFPS cycles, a Lane Adapter in CL1 or CL2 state shall: 2. Return to Electrical Idle for tPreData.
4.2.1.6.5.2#10	TD 4.010 TD 4.012	Upon detecting 2 LFPS cycles, a Lane Adapter in CL1 or CL2 state shall: 3. Start transmitting SLOS1 on the Lane.

4.2.1.6.5.2#11	TD 4.010 TD 4.012	Upon detecting 2 LFPS cycles, a Lane Adapter in CL1 or CL2 state shall: 4. Enable the receiver to start bit and symbol synchronization not earlier than tCLxIdleRx after the last LFPS cycle received. A Lane Adapter shall complete Symbol lock within tRxLock time.
4.2.1.6.5.2#12	TD 4.010 TD 4.012	Upon detecting 2 LFPS cycles, a Lane Adapter in CL1 or CL2 state shall: 5. Transition to Training.LOCK1 sub-state.
4.2.1.6.5.2#13	TD 4.010 TD 4.012	On transition to the TS1 sub-state, the USB4 Port shall enable SSC if SSC is disabled
<b>4.2.1.6.5.3 Exit Flow from CL1 or CL2 State (Re-timers on the Link)</b>		
4.2.1.6.5.3#1	TD 4.016	The USB4 Port initiating exit from CL1 or CL2 state shall: 1. Send a Low Frequency Periodic Signaling (LFPS) burst on each Lane until its receiver detects LFPS.
4.2.1.6.5.3#2	TBD	If the receiver did not detect LFPS after tTrainingAbort2 time the Router shall initiate a Disconnect by driving SBTx to a logical low state for tDisconnectTx.
4.2.1.6.5.3#3	TD 4.016	The USB4 Port initiating exit from CL1 or CL2 state shall: 2. Return to Electrical Idle for tPreData.
4.2.1.6.5.3#4	TD 4.016	The USB4 Port initiating exit from CL1 or CL2 state shall: 3. Start transmitting SLOS1 on the Lane.
4.2.1.6.5.3#5	TD 4.016	The USB4 Port initiating exit from CL1 or CL2 state shall: 4. Enable the receiver to start bit and symbol synchronization not earlier than tCLxIdleRx after the last LFPS cycle received. A Lane Adapter shall complete Symbol lock within tRxLock time.
4.2.1.6.5.3#6	TD 4.016	The USB4 Port initiating exit from CL1 or CL2 state shall: 5. Upon reception of 3 back-to-back CL_WAKE1.X Ordered Set Symbols, start transmitting CL_WAKE2.X Ordered Set Symbols on the Lane. The Adapter shall ignore any received CL_WAKE2.Y (where Y is any value) Symbols interleaved with CL_WAKE1.X Ordered Set SymbolCL_WAKE1.X Ordered Set Symbols when it determines the reception of back-to-back CL_WAKE1.X Ordered Set SymbolCL_WAKE1.X Ordered Set Symbols.
4.2.1.6.5.3#7	TD 4.016	The USB4 Port initiating exit from CL1 or CL2 state shall: 6. Upon reception of 7 back-to-back CL_WAKE2.X Ordered Set Symbols or 7 back-to-back SLOS Symbols, transition the Adapter to Training.LOCK1 sub-state within tWakeResponse time.
4.2.1.6.5.3#8	NT	On transition to the TS1 sub-state, the USB4 Port shall enable SSC if SSC is disabled.

4.2.1.6.5.3#9	TD 4.011 TD 4.013	Upon detecting 2 LFPS cycles, a Lane Adapter in CL1 or CL2 state shall: 1. Send a Low Frequency Periodic Signaling (LFPS) burst on the Lane for the duration of at least 3 LFPS cycles and for no more than tLFPSDuration. If the Lane Adapter is in CL1 state, the first LFPS shall be sent within tWarmUpCL1 after receiving the first LFPS cycle. If the Lane Adapter is in CL2 state, the first LFPS shall be sent within tWarmUpCL2 after receiving the first LFPS cycle.
4.2.1.6.5.3#10	TD 4.011 TD 4.013	Upon detecting 2 LFPS cycles, a Lane Adapter in CL1 or CL2 state shall: 2. Return to Electrical Idle for tPreData.
4.2.1.6.5.3#11	TD 4.011 TD 4.013	Upon detecting 2 LFPS cycles, a Lane Adapter in CL1 or CL2 state shall: 3. Start transmitting SLOS1 on the Lane.
4.2.1.6.5.3#12	TD 4.011 TD 4.013	Upon detecting 2 LFPS cycles, a Lane Adapter in CL1 or CL2 state shall: 4. Enable the receiver to start bit and symbol synchronization not earlier than tCLxIdleRx after the last LFPS cycle received. An Adapter shall complete Symbol lock within tRxLock time.
4.2.1.6.5.3#13	TD 4.011 TD 4.013	Upon detecting 2 LFPS cycles, a Lane Adapter in CL1 or CL2 state shall: 5. Upon reception of 3 back-to-back CL_WAKE1.X Ordered Set Symbols, start transmitting CL_WAKE2.X Ordered Set Symbols on the Lane. The Adapter shall ignore any received CL_WAKE2.Y (where Y is any value) Symbols interleaved with CL_WAKE1.X Ordered Set Symbols when it determines the reception of back-to-back CL_WAKE1.X Ordered Set Symbols.
4.2.1.6.5.3#14	TD 4.011 TD 4.013	Upon detecting 2 LFPS cycles, a Lane Adapter in CL1 or CL2 state shall: 6. Upon reception of 7 back-to-back CL_WAKE2.X Ordered Set Symbols or 7 back-to-back SLOS Symbols, transition to Training.LOCK1 sub-state.
4.2.1.6.5.3#15	TD 4.011 TD 4.013	On transition to the TS1 sub-state, the USB4 Port shall enable SSC if SSC is disabled.
<b>4.2.2 USB4 Link Transitions</b>		
4.2.2#1	IOP	A USB4 Link shall operate as either a Single-Lane Link or a Dual-Lane Link.
<b>4.2.2.1 Transition from One Single-Lane Link to Two Single-Lane Links</b>		
4.2.2.1#1	NT	A USB4 Port shall transition from one single-Lane Link to two single-Lane Links when the Lane 1 Adapter is enabled.
<b>4.2.2.2 Transition from Two Single-Lane Link to Dual-Lane Link</b>		
4.2.2.2#1	TD 4.005	A USB4 Port shall transition its Lane Adapters to the Lane Bonding state when all of the following are true: Both Ports are in the Bonding state; The Supported Link Widths field of both Ports is set to x2 support or more; The Target Link Width field of both Ports is set to establish a dual-Lane Link.

4.2.2.2#2	TD 4.005	The Logical Layer shall transition to a Dual-Lane Link when the following conditions are met: Both Adapters have transitioned successfully to CL0 state within tBonding time after sending the first TS1 Ordered Set with <i>Lane Bonding Target</i> set to 001b ; Link Partner has responded with the following value in all TS1 and TS2 Ordered Sets on both Lanes (Lane Bonding Target is set to 001b).
4.2.2.2#3	TD 4.005	If Lane bonding is successful, then a Router shall set the Adapter State field in the Lane Adapter Configuration Capability of the Lane 0 Adapter to CL0.
4.2.2.2#4	TD 4.005	If Lane bonding is successful, then a Router shall set the Negotiated Link Width field in the Lane Adapter Configuration Capability of the Lane 0 Adapter to indicate a USB4 Link width of x2.
4.2.2.2#5	TD 4.005	If Lane bonding is successful, then a Router shall send a Hot Plug Event Packet with the UPG bit set to 1b for the Lane 1 Adapter in the Downstream Facing Port.
4.2.2.2#6	TD 4.035	If one of the Lane Adapters is not in CL0 tBonding time after entry to the Lane Bonding state, the Router shall initiate a Disconnect by driving SBTx to a logical low state for tDisconnectTx.
4.2.2.2#7	TD 4.020	The Adapters of a dual-Lane Link operate in CL0 state in tandem with the following dependencies: Any Ordered Set sent on the Link shall be sent simultaneously on both Lanes within the permitted transmit skew.
4.2.2.2#8	BC	The Adapters of a dual-Lane Link operate in CL0 state in tandem with the following dependencies: When either Adapter of a dual-Lane Link transitions to one of the Training sub-states, the other Adapter in the USB4 Port shall transition to the same Training sub-state.
<b>4.2.2.2.1 Training a Dual-Lane Link</b>		
4.2.2.2.1#1	TD 4.040 TD 4.041	When an Adapter that is part of a dual-Lane Link enters Training state, the other Adapter in the USB4 Port shall enter Training state as well.
4.2.2.2.1#2	TD 4.009	The Logical Layer shall resume dual-Lane Link operation if both Ports meet the transition conditions in Step 6 of the Training state machine in Table 4-20 within tTrainingAbort2 time.
4.2.2.2.1#3	TD 4.009	The Adapter that transitions to the CL0 state first shall send TS2 Ordered Sets until the other Adapter in the USB4 Port exits the training state.
<b>4.2.2.3 Transition from Dual-Lane Link to Two Single-Lane Links</b>		
<b>4.2.2.4 Transition from Two Single-Lane Links to One Single Lane Link</b>		
4.2.2.4#1	TD 4.006	A USB4 Port shall transition from two Single-Lane Links to one Single-Lane Link when one of its Adapters transitions to the Disabled state.

<b>4.2.3 Logical Layer Link States</b>		
<b>4.3 USB4 Link Encoding</b>		
4.3#1	IOP	If RS_FEC encoding is off, bytes received from the Transport Layer shall be encoded with either 64b/66b encoding (Gen 2) or 128b/132b encoding (Gen 3)
<b>4.3.1 Lane Distribution</b>		
4.3.1#1	IOP	If a USB4 Link operates as a dual-Lane Link, then distribution of Transport Layer bytes among the Lanes shall alternate as depicted in Figure 4-13.
<b>4.3.2 Symbol Encoding</b>		
<b>4.3.2.1 Symbol Encoding of Transport Layer Bytes</b>		
4.3.2.1#1	NT	A Symbol may contain either Transport Layer bytes or Ordered Set, but shall not contain both
<b>4.3.3 Ordered Sets</b>		
4.3.3#1	IOP	Ordered Set shall have the structure depicted in Table 4-35.
4.3.3#2	IOP	For 64b/66b encoding, an Ordered Set Symbol shall contain a single copy of the Ordered Set payload and 2 Sync Bits.
4.3.3#3	IOP	For 128b/132b encoding, an Ordered Set Symbol shall contain two copies of the Ordered Set (i.e. 64 bits followed by a second copy of the same 64 bits) and 4 Sync Bits.
<b>4.3.4 Bit Swap</b>		
4.3.4#1	IOP	Bit Swap of Transport Layer bytes and of Ordered Sets payload delivered to the scrambler in the order that they are transmitted on the wire.
<b>4.3.4.1 Sync Bits</b>		
4.3.4.1#1	IOP	If RS-FEC is off, all Symbols shall be transmitted Sync Bits first.
4.3.4.1#2	IOP	Sync Bits shall be sent in the order of most significant bit to least significant bit.
4.3.4.1#3	IOP	Transport Layer bytes or Ordered Sets shall be transmitted after the Sync Bits.
<b>4.3.4.2 Data Symbol Payload</b>		
4.3.4.2#1	IOP	The payload within a Data Symbol shall be transmitted from left to right as depicted in Figure 4-18.
4.3.4.2#2	IOP	Within each byte of payload, individual bits shall be transmitted from bit 0 to bit 7.

4.3.4.3 Ordered Set Symbol Payload		
4.3.4.3#1	IOP	When an Ordered Set is longer than 64 bits (i.e. SLOS, CL_WAKE1.X, CL_WAKE2.X), it cannot fit into the payload of one Symbol, and shall be divided into multiple Symbol payloads.
4.3.4.3#2	IOP	The Ordered Set shall be transmitted in increasing Symbols, starting with Symbol 0.
4.3.4.3#3	IOP	Within a Symbol payload, the bytes in an Ordered Set shall be transmitted from left to right as depicted in Figure 4-19.
4.3.4.3#4	IOP	Within each byte, individual bits shall be transmitted from bit 0 to bit 7.
4.3.5 Scrambling		
4.3.5#1	IOP	Scrambling shall be performed according to the rules in Table 4-36.
4.3.5#2	IOP	Scrambling and de-scrambling are performed by passing the encoded bits through an Additive LFSR with a polynomial of $G(X) = X^{23} + X^{21} + X^{16} + X^8 + X^5 + X^2 + 1$ .
4.3.5#3	IOP	The most significant bit of the LFSR is XORed with the data stream on a per-bit basis. The data stream is scrambled in the order that it is sent on wire.
4.3.5#4	IOP	The scrambler shall load a new seed on the following transitions: 1. Transition from LOCK2 sub-state to TS1 sub-state in the Training state; Initial value is 1F EEDDh.
4.3.5#5	IOP	The scrambler shall load a new seed on the following transitions: 2. On exit from CL0s state, before the Adapter initiating exit transmits the first TS2 Ordered Set in the direction exiting electrical idle; Initial value is 1F EEDDh.
4.3.5#6	IOP	The scrambler shall load a new seed on the following transitions: 3. On transition from any state to CL0 when going to a dual-Lane Link; When exiting CL0s state, a new seed shall be loaded only in the direction exiting electrical idle; Initial value on the Lane 0 is 1D BFBCh; Initial value on the Lane 1 is 06 07BBh; The per-Lane seeds are used, starting with the first byte after the de-skew Ordered Set.
4.3.5#8	IOP	Any single-bit errors in the SRC field shall be corrected. If the SCR field contains an uncorrectable error, the Logical Layer reports an OSE error.
4.3.6 RS-FEC		
4.3.6#1	IOP	An Adapter shall support RS-FEC at all speeds.
4.3.6#2	IOP	Each block of 194 bytes shall be generated in the following manner: Transport Layer bytes and Ordered Sets are grouped into 16-byte (128 bit) Symbol payloads. Each Symbol payload may contain either one or more Ordered Set or Transport Layer bytes, but shall not contain both.

4.3.6#3	IOP	Each block of 194 bytes shall be generated in the following manner: When operating at Gen 2 speed, the 16-byte Ordered Set Symbol payload shall contain: For a SLOS Ordered Set, 128 bits of the Ordered Set.
4.3.6#4	IOP	Each block of 194 bytes shall be generated in the following manner: When operating at Gen 2 speed, the 16-byte Ordered Set Symbol payload shall contain: For all other Ordered Sets, two 64-bit Ordered Sets.
4.3.6#5	IOP	When only one Ordered Set needs to be sent, the second Ordered Set shall be a SKIP Ordered Set. See Section 4.4.3 for the structure of a SKIP Ordered Set.
4.3.6#6	IOP	Each block of 194 bytes shall be generated in the following manner: When operating at Gen 3 speed, the 16-byte Ordered Set Symbol payload shall contain: For a SLOS Ordered Set, 128 bits of the Ordered Set.
4.3.6#7	IOP	Each block of 194 bytes shall be generated in the following manner: When operating at Gen 3 speed, the 16-byte Ordered Set Symbol payload shall contain: For all other Ordered Sets, two copies of the Ordered Set (i.e. 64 bits followed by a second copy of the same 64 bits).
4.3.6#8	IOP	Each block of 194 bytes shall be generated in the following manner: The RS-FEC encoder is fed with twelve 16-byte Symbol payloads plus 2 bytes of Sync Bits. Each Symbol is allocated a single Sync Bit, indicating whether it contains Transport Layer bytes (Sync Bit = 0b) or Ordered Set (Sync Bit = 1b).
4.3.6#9	IOP	The 2 bytes of Sync Bits contain 12 active bits (one per 16-byte Symbol) and 4 reserved bits.
4.3.6#10	IOP	Sync Bits shall be delivered to the encoder in order that they will be sent to the wire, from bit 15 to bit 0. The active Sync Bits reside in bits[11:0] of the Word. The Sync Bit corresponding to the oldest 16-byte Symbol resides in bit 0 if the Sync Bits.
4.3.6#11	IOP	The 12 active bits are XORed with 333h before being fed to the RS-FEC encoder. The XORed value is the value seen on the wire.
4.3.6#12	IOP	Each block of 194 bytes shall be generated in the following manner: The RS-FEC encoder generates 4 bytes of redundancy bits (P3 to P0). P3 is the first byte to be sent on the wire and P0 is the last. Within each byte, bits are sent in descending order where bit 7 is sent first and bit 0 is sent last.
4.3.6#13	TD 4.039	The RS-FEC decoder shall correct a received block with up to two 1-byte errors anywhere in the block.
4.3.6#14	NT	An error in a received block that is detectable and uncorrectable shall cause an RDE error.

<b>4.3.6.1 RS_FEC Activation and Deactivation</b>		
4.3.6.1#1	IOP	If RS-FEC is enabled during Phase 3 of Lane Initialization, then an Adapter shall activate RS-FEC encoding in the following cases: In Training state, immediately following the last transmitted SLOS2 and before sending the first TS1 Ordered Set.
4.3.6.1#2	IOP	If RS-FEC is enabled during Phase 3 of Lane Initialization, then an Adapter shall activate RS-FEC encoding in the following cases: During exit from CL0s state, immediately before sending the first TS2 Ordered Set.
4.3.6.1#3	IOP	A START_RS_FEC bit sequence shall be sent prior to activating RS-FEC encoding on the Lane.
4.3.6.1#4	IOP	The bit sequence shall not be scrambled and shall not advance the scrambler LFSR.
4.3.6.1#5	IOP	The START_RS_FEC bit sequence shall be sent with bit[31] first on the wire.
4.3.6.1#6	IOP	During exit from CL0s state, the START_RS_FEC bit sequence shall only be sent in the direction exiting electrical idle.
4.3.6.1#7	IOP	The bit following the START_RS_FEC bit sequence shall be the first bit to be RS-FEC encoded.
4.3.6.1#8	IOP	If RS-FEC encoding is activated, a USB4 Port shall deactivate RS-FEC encoding on a Lane in the following cases: When to Training state, after transmitting n SLOS1 Symbols in LOCK1 sub-state with RS-FEC on, where $32 \leq n \leq 64$ in Gen 2 and $16 \leq n \leq 32$ in Gen 3.
4.3.6.1#9	IOP	If RS-FEC encoding is activated, a USB4 Port shall deactivate RS-FEC encoding on a Lane in the following cases: Entry to Disabled state.
4.3.6.1#10	IOP	If RS-FEC encoding is activated, a USB4 Port shall deactivate RS-FEC encoding on a Lane in the following cases: Entry to CLd state.
4.3.6.1#11	IOP	If RS-FEC encoding is activated, a USB4 Port shall deactivate RS-FEC encoding on a Lane in the following cases: Entry to CL0s state, in the direction entering low power state.
4.3.6.1#12	IOP	If RS-FEC encoding is activated, a USB4 Port shall deactivate RS-FEC encoding on a Lane in the following cases: Entry to CL2 or CL1 states.
4.3.6.1#13	IOP	If RS-FEC encoding is activated, a USB4 Port shall deactivate RS-FEC encoding on a Lane in the following cases: Entry to Training.LOCK2 sub-state.
<b>4.3.6.2 Pre-Coding</b>		
4.3.6.2#1	IOP	If pre-coding is on, then before each bit is sent on the wire, it shall be XOR'ed with the bit sent before it, using the value of the bit after it was coded.



4.3.6.2#2	IOP	Pre-coding shall be turned on with the first bit that is RS_FEC encoded.
4.3.6.2#3	IOP	Pre-coding shall be turned off with the first bit that is not RS_FEC encoded.
<b>4.4 USB4 Link Operation</b>		
<b>4.4.1 Start of Data</b>		
4.4.1#1	BC	When an Adapter transitions to CL0 state, the first transmitted bytes after the last TS2 Ordered Set shall be either a Transport Layer header, an Idle Packet or any Ordered Set other than SLOS, TS1 or TS2.
4.4.1#2	BC	For a dual-Lane Link, the first transmitted bytes after the last TS2 Ordered Set shall be a de-skew Ordered Set followed by either a Transport Layer header, an Idle Packet or any Ordered Set other than SLOS, TS1 or TS2.
<b>4.4.2 Error Cases and Recovery</b>		
4.4.2#32	TD 4.040	A Router shall support the Ordered Set Errors (OSE) error case.
4.4.2#33	TD 4.040	When a Router supports an error case, it shall do so as described in this section.
4.4.2#34	TD 4.040	A Router shall support the same error cases on all Lane Adapters.
4.4.2#35	TD 4.040	When an Adapter supports an error case, it shall support that error case in all Adapter states unless specified otherwise.
4.4.2#36	NT	If an Adapter reports Alignment Lock Errors, when an Adapter receives N number of Symbols in a row with illegal Sync Bits values, where N is a number between 1 and 8 (inclusive) that is chosen by the implementation, it shall go to Training.LOCK1 sub-state.
4.4.2#37	NT	If an Adapter reports Alignment Lock Errors, when an Adapter receives a Symbol with illegal Sync bit values, it shall set the ALE bit in the Logical Layer Errors field to 1b.
4.4.2#38	NT	If an Adapter reports Alignment Lock Errors, when an Adapter receives a Symbol with illegal Sync bit values, if the ALE bit in the Logical Layer Errors Enable field is 1b, the Router shall send a Notification Packet with Event Code = ERR_LINK to the Connection Manager.
4.4.2#39	NT	If an Adapter reports Alignment Lock Errors, when an Adapter receives a Symbol with illegal Sync bit values, if the ALE bit in the Logical Layer Errors Enable field is 0b, the Router shall not send a Notification Packet.
4.4.2#40	TD 4.040	If an Adapter reports Ordered Set Errors, when it receives 2 back-to-back Symbols that contain an Ordered Set that is not defined in this specification and/or have an uncorrectable error in the SRC field, it shall go to Training.LOCK1 sub-state.

4.4.2#41	TD 4.040 TD 4.041	If an Adapter reports Ordered Set Errors, when it receives 2 back-to-back Symbols that are not part of an Ordered Set defined in this specification and/or have an uncorrectable error in the SRC field, it shall set the OSE bit in the Logical Layer Errors field to 1b.
4.4.2#42	TD 4.040 TD 4.041	If an Adapter reports Ordered Set Errors, when it receives 2 back-to-back Symbols that are not part of an Ordered Set defined in this specification and/or have an uncorrectable error in the SRC field, if the OSE bit in the Logical Layer Errors Enable field is 1b, the Router shall send a Notification Packet with Event Code = ERR_LINK to the Connection Manager.
4.4.2#43	TD 4.040 TD 4.041	If an Adapter reports Ordered Set Errors, when it receives 2 back-to-back Symbols that are not part of an Ordered Set defined in this specification and/or have an uncorrectable error in the SRC field, if the OSE bit in the Logical Layer Errors Enable field is 0b, the Router shall not send a Notification Packet.
4.4.2#44	NT	If an Adapter reports Timeout Errors, when an Adapter entered Training state from either CL0, CL1, or CL2 state and did not transition to CL0 state within tTrainingError after sending the first SLOS1.
4.4.2#45	NT	If an Adapter reports Timeout Errors, when an Adapter does not transition from Training state to CL0 state within tTrainingError after achieving Symbol alignment, it shall set the TE bit in the Logical Layer Errors field to 1b.
4.4.2#46	TD 4.042	If an Adapter reports Timeout Errors, when an Adapter does not transition from Training state to CL0 state within tTrainingError after achieving Symbol alignment, if the TE bit in the Logical Layer Errors Enable field is 1b, the Router shall send a Notification Packet with Event Code = ERR_LINK to the Connection Manager.
4.4.2#47	TD 4.042	If an Adapter reports Timeout Errors, when an Adapter does not transition from Training state to CL0 state within tTrainingError after achieving Symbol alignment, if the TE bit in the Logical Layer Errors Enable field is 0b, the Router shall not send a Notification Packet.
4.4.2#48	NT	If an Adapter reports Elastic Buffer Errors, when the elastic buffer is full, it shall: go to Training.LOCK1 sub-state.
4.4.2#49	NT	If an Adapter reports Elastic Buffer Errors, when the elastic buffer is full, it shall set the EBE bit in the Logical Layer Errors field to 1b.
4.4.2#50	NT	If an Adapter reports Elastic Buffer Errors, when the elastic buffer is full, if the EBE bit in the Logical Layer Errors Enable field is 1b, the Router shall send a Notification Packet with Event Code = ERR_LINK to the Connection Manager (see Section 6.5).
4.4.2#51	NT	If an Adapter reports Elastic Buffer Errors, when the elastic buffer is full, if the EBE bit in the Logical Layer Errors Enable field is 0b, the Router shall not send a Notification Packet.

4.4.2#52	NT	If an Adapter reports De-skew Buffer Errors, when skew is too large resulting in overflow in the de-skew buffer, it shall set the DBE bit in the Logical Layer Errors field to 1b.
4.4.2#53	NT	If an Adapter reports De-skew Buffer Errors, when skew is too large resulting in overflow in the de-skew buffer, if the DBE bit in the Logical Layer Errors Enable field is 1b, the Router shall send a Notification Packet with Event Code = ERR_LINK to the Connection Manager.
4.4.2#54	NT	If an Adapter reports De-skew Buffer Errors, when skew is too large resulting in overflow in the de-skew buffer, if the DBE bit in the Logical Layer Errors Enable field is 0b, the Router shall not send a Notification Packet.
4.4.2#55	NT	If an Adapter reports RS-FEC decoder errors, when the RS-FEC decoder identifies an uncorrectable error, it shall turn off RS-FEC in both directions of the Link.
4.4.2#56	NT	If an Adapter reports RS-FEC decoder errors, when the RS-FEC decoder identifies an uncorrectable error, it shall set the RDE bit in the Logical Layer Errors field to 1b.
4.4.2#57	NT	If an Adapter reports RS-FEC decoder errors, when the RS-FEC decoder identifies an uncorrectable error, if the RDE bit in the Logical Layer Errors Enable field is 1b, the Router shall send a Notification Packet with Event Code = ERR_LINK to the Connection Manager.
4.4.2#58	NT	If an Adapter reports RS-FEC decoder errors, when the RS-FEC decoder identifies an uncorrectable error, if the RDE bit in the Logical Layer Errors Enable field is 0b, the Router shall not send a Notification Packet.
4.4.2#59	NT	If an Adapter reports RX Sync Timeout, if, while in LOCK1 sub-state of the Training state, the receiver cannot lock on Sync Bits for an implementation-specific period of time, it shall remain in LOCK1 sub-state.
4.4.2#60	NT	If an Adapter reports RX Sync Timeout, if, while in LOCK1 sub-state of the Training state, the receiver cannot lock on Sync Bits for an implementation-specific period of time, it shall set the RST bit in the Logical Layer Errors field to 1b.
4.4.2#61	NT	If an Adapter reports RX Sync Timeout, if, while in LOCK1 sub-state of the Training state, the receiver cannot lock on Sync Bits for an implementation-specific period of time, if the RST bit in the Logical Layer Errors Enable field is 1b, the Router shall send a Notification Packet with Event Code = ERR_LINK to the Connection Manager.
4.4.2#62	NT	If an Adapter reports RX Sync Timeout, if, while in LOCK1 sub-state of the Training state, the receiver cannot lock on Sync Bits for an implementation-specific period of time, if the RST bit in the Logical Layer Errors Enable field is 0b, the Router shall not send a Notification Packet.

<b>4.4.3 Clock Compensation and SKIP</b>		
4.4.3#1	IOP	A receiver shall drop any received SKIP Ordered Sets and shall be capable of operating in the absence of any SKIP Ordered sets.
4.4.3#2	IOP	A Transmitter shall not send SKIP Ordered Sets while the Adapter is in the Training.LOCK1 or Training.LOCK2 sub-states.
4.4.3#3	IOP	A SKIP Ordered Set shall have the structure defined in Table 4-39.
4.4.3#4	IOP	SCR – Shall be set to 11 0000 1101b to indicate that the Ordered Set contents are not scrambled.
<b>4.4.4 Dual-Lane Skew</b>		
4.4.4#11	TD 4.043	A Router shall operate with skew defined in Section 3.5.1 between the receiving Lanes of a Link when measured at the USB Type-C connector.
4.4.4#12	NT	A transmitter shall not introduce skew more than defined in Section 3.4.1.
4.4.4#13	TD 4.009	A single de-skew Ordered Set shall be sent on each Lane after both Adapters transition (from any state) to CL0 state, and the USB4 Port in Dual-Lane Link mode.
4.4.4#14	TD 4.009	When exiting CL0s state, a de-skew Ordered Set shall only be sent in the direction exiting electrical idle.
4.4.4#15	TBD	When a Port operates at Gen 3 speed, the De-Skew Ordered Set shall be transmitted twice. Otherwise it shall be transmitted once.
4.4.4#16	TD 4.009	A de-skew Ordered Set shall be sent simultaneously on both Lanes within the permitted transmit skew
4.4.4#17	TD 4.009	A de-skew Ordered Set shall be sent on both Lanes in the same locations within the Symbol.
4.4.4#18	TD 4.009	The de-skew Ordered Set shall be the first bytes sent after the TS2 Ordered Sets.
4.4.4#19	TD 4.009	TS2 Ordered Sets shall be transmitted on a Lane in CL0 state until the de-skew Ordered Set is sent.
4.4.4#20	NT	SCR in the De-Skew Ordered Set payload shall be set to 00 1111 0010b to indicate that the Ordered Set contents are scrambled.

<b>4.4.5 Disconnect</b>		
<b>4.4.5.1 Upstream Facing Port Disconnect</b>		
<b>4.4.5.1.1 SBRX Goes Low</b>		
4.4.5.1.1#1	TD 4.017	The Router with the disconnected Port shall: Drive SBTX to a logical low state on all USB4 Ports for tDisconnectTx.
4.4.5.1.1#2	TD 4.017	The Router with the disconnected Port shall: Transition to the Uninitialized Unplugged state.
4.4.5.1.1#3	CH6	The following events initiate a disconnect as defined in this section: Router Hot Unplug.
4.4.5.1.1#4	CH6	The following events initiate a disconnect as defined in this section: Downstream Facing Port Reset where the Link Partner is an Upstream Facing Port.
4.4.5.1.1#5	TD 4.017	The following events initiate a disconnect as defined in this section: The Domain enters Sleep state, the USB4 Port is Configured bit in a USB4 Port is set to 0b, and the Link Partner is an Upstream Facing Port.
4.4.5.1.1#6	TBD	The following events initiate a disconnect as defined in this section: The Link Partner failed to train the Link before the defined timeout.
4.4.5.1.1#7	TBD	The following events initiate a disconnect as defined in this section: The Lane bonding did not complete before the defined timeout.
<b>4.4.5.1.2 LT_Fall Transaction is Received</b>		
<b>4.4.5.1.3 LT_LRoff Transaction is Received on an Upstream Facing Port</b>		
4.4.5.1.3#1	NT	When an Upstream Facing Port receives an LT_LRoff transaction and the <i>Enter Sleep</i> bit in the Router Configuration Space is set to 0b, the Port is disconnected. The disconnected Port shall send an LT_LRoff Transaction.
4.4.5.1.3#2	NT	The Router with the disconnected Port shall: Drive SBTX to a logical low state on all USB4 Ports for tDisconnectTx.
4.4.5.1.3#3	NT	The Router with the disconnected Port shall: Transition to the Uninitialized Unplugged state.
4.4.5.1.3#4	NT	The following events shall initiate a disconnect as defined in this section: The Domain enters Sleep state, in the Downstream Facing Port of the Link Partner the USB4 Port is Configured bit is 0b and the Enable Wake on Connect bit of the USB4 Port is 1b.

4.4.5.2 Downstream Port Disconnect		
4.4.5.2.1 SBRX Goes Low		
4.4.5.2.1#1	TD 4.018	When a Downstream Facing Port detects SBRX at logical low state for tDisconnectRx and its <i>Lane Disable</i> bit in the Lane 0 Adapter Configuration Capability is set to 0b, the Port is disconnected and shall: Send an LT_LRoff Transaction.
4.4.5.2.1#2	TD 4.018	When a Downstream Facing Port detects SBRX at logical low state for tDisconnectRx and its <i>Lane Disable</i> bit in the Lane 0 Adapter Configuration Capability is set to 0b, the Port is disconnected and shall: Discard any Transport Layer Packets received from the Ingress Port(s) on the Router.
4.4.5.2.1#3	TD 4.018	When a Downstream Facing Port detects SBRX at logical low state for tDisconnectRx and its <i>Lane Disable</i> bit in the Lane 0 Adapter Configuration Capability is set to 0b, the Port is disconnected and shall: Transition its Adapters to the CLd state
4.4.5.2.1#4	NT	The Router with the disconnected Port shall continue to send flow control Packets on the Ingress Port(s) for Transport Layer Packets that the disconnected Port discarded.
4.4.5.2.1#5	NT	Flow control credit counts shall be updated as if the discarded packets were dequeued and forwarded to the Egress Adapter.
4.4.5.2.1#6	TD 4.018	The Router shall do the following for each enabled Lane Adapter in the disconnected Port: Send the Connection Manager a Hot Plug Event Packet with the <i>UPG</i> bit set to 1b.
4.4.5.2.1#7	TD 4.018	The Router shall do the following for each enabled Lane Adapter in the disconnected Port: Load the following fields in the Adapter Configuration Space with their default values: Basic Configuration Registers: Link Credits Allocated; TMU Adapter Configuration Capability: Inter-Domain Time Initiator, EnableUniDirectionalMode; Lane Adapter Configuration Capability: Target Link Width, CL0s Enable, CL1 Enable, CL2 Enable, Lane Bonding.
4.4.5.2.1#8	NT	The Router shall do the following for each enabled Lane Adapter in the disconnected Port: Load the TxFFE register in the SB Register Space with its default values.
4.4.5.2.2 LT_LRoff Transaction is Received		
4.4.5.2.2#1	NT	When a Downstream Facing Port receives an LT_LRoff Transaction and the <i>Enter Sleep</i> bit in the Router Configuration Space is set to 0b, the Port is disconnected and shall: Send an LT_LRoff Transaction.
4.4.5.2.2#2	NT	When a Downstream Facing Port receives an LT_LRoff Transaction and the <i>Enter Sleep</i> bit in the Router Configuration Space is set to 0b, the Port is disconnected and shall: Discard any Transport Layer Packets received from the Ingress Port(s) on the Router.

4.4.5.2.2#3	NT	When a Downstream Facing Port receives an LT_LRoff Transaction and the <i>Enter Sleep</i> bit in the Router Configuration Space is set to 0b, the Port is disconnected and shall: Transition its Adapters to the CLd state.
4.4.5.2.2#4	NT	The Router with the disconnected Port shall continue to send flow control Packets on the Ingress Port(s) for Transport Layer Packets that the disconnected Port discarded.
4.4.5.2.2#5	NT	Flow control credit counts shall be updated as if the discarded packets were dequeued and forwarded to the Egress Adapter.
4.4.5.2.2#6	NT	The Router shall do the following for each enabled Lane Adapter in the disconnected Port: Send the Connection Manager a Hot Plug Event Packet with the UPG bit set to 1b.
4.4.5.2.2#7	NT	The Router shall do the following for each enabled Lane Adapter in the disconnected Port: Load the following fields in Adapter Configuration Space with their default values: Basic Configuration Registers: Link Credits Allocated; TMU Adapter Configuration Capability: Inter-Domain Time Initiator, EnableUniDirectionalMode; Lane Adapter Configuration Capability: Target Link Width CL0s Enable CL1 Enable CL2 Enable Lane Bonding.
4.4.5.2.2#8	NT	The Router shall do the following for each enabled Lane Adapter in the disconnected Port: Load the TxFFE register in SB Register Space with its default values.
4.4.5.2.2#9	NT	The Router shall do the following for each enabled Lane Adapter in the disconnected Port: Start Lane Initialization from Phase 2.
<b>4.4.6 Lane Adapter Disable and Enable</b>		
<b>4.4.6.1 Disabled Adapter is the Upstream Adapter</b>		
4.4.6#1	NT	After the <i>Lane Disable</i> bit in its Upstream Adapter is set to 1b, a Router shall: 1. Send an LT_Fall Transaction to the Link Partner of the Upstream Facing Port to signal transition to the Disabled state.
4.4.6#2	NT	After the <i>Lane Disable</i> bit in its Upstream Adapter is set to 1b, a Router shall: 2. Drive SBTx to a logical low state on all USB4 Ports for tDisconnectTx.
4.4.6#3	NT	After the <i>Lane Disable</i> bit in its Upstream Adapter is set to 1b, a Router shall: 3. Transition to the Uninitialized Unplugged state.
4.4.6#4	NT	After the <i>Lane Disable</i> bit in its Upstream Adapter is set to 1b, a Router shall: 4. Start Lane Initialization from Phase 1.
4.4.6#5	NT	After the <i>Lane Disable</i> bit in its Upstream Adapter is set to 1b, a Router shall: 5. After detecting a Router on the Upstream Facing Port, transition to the Uninitialized Plugged state.

4.4.6.2 Disabled Adapter is not the Upstream Adapter		
4.4.6.2.1 Disable Flow		
4.4.6.2.1#1	TD 4.006	After the <i>Lane Disable</i> bit in the Adapter Configuration Space of the Lane Adapter is set to 1b, the Router shall: 1. Send an LT_Fall Transaction to the Link Partner of the Upstream Facing Port to signal transition to the Disabled state.
4.4.6.2.1#2	TD 4.006	After the <i>Lane Disable</i> bit in the Adapter Configuration Space of the Lane Adapter is set to 1b, the Router shall: 2. Send a Hot Plug Event Packet for the disabled Adapter with the UPG bit set to 1b to the Connection Manager.
4.4.6.2.1#3	TD 4.006	After the <i>Lane Disable</i> bit in the Adapter Configuration Space of the Lane Adapter is set to 1b, the Router shall: 3. Transition the Adapter to the Disabled State.
4.4.6.2.1#4	NT	After the <i>Lane Disable</i> bit in the Adapter Configuration Space of the Lane Adapter is set to 1b, the Router shall: 4. If the Router detects that SBRX of the disabled Adapter transitions to a low logical state for more than tDisconnectRx, the Router shall perform the disconnect flow defined in Section 4.4.5.2.1.
4.4.6.2.1.1 Link Partner is not the Upstream Adapter		
4.4.6.2.1.1#1	TD 4.007	If the Link Partner of the disabled Adapter is not the Upstream Adapter, it shall do the following upon receiving the LT_Fall Transaction: 1. Send a Hot Plug Event Packet with the UPG bit set to 1b to the Connection Manager.
4.4.6.2.1.1#2	TD 4.006 TD 4.007	If the Link Partner of the disabled Adapter is not the Upstream Adapter, it shall do the following upon receiving the LT_Fall Transaction: 2. Load the following fields in the Adapter Configuration Space of the Adapter with their default values: Basic Configuration Registers: Link Credits Allocated; TMU Adapter Configuration Capability: Inter-Domain Time Initiator; USB4 Port Configuration Capability: Target Link Width CL0s Enable CL1 Enable CL2 Enable Lane Bonding.
4.4.6.2.1.1#3	NT	If the Link Partner of the disabled Adapter is not the Upstream Adapter, it shall do the following upon receiving the LT_Fall Transaction: 3. Transition to the CLd state.
4.4.6.2.1.2 Link Partner is the Upstream Adapter		
4.4.6.2.1.2#1	TD 4.007	If the Link Partner of the disabled Adapter is the Upstream Adapter, it shall do the following upon receiving the LT_Fall Transaction: 1. Drive SBTx to a logical low state on all USB4 Ports for tDisconnectTx.
4.4.6.2.1.2#2	TD 4.007	If the Link Partner of the disabled Adapter is the Upstream Adapter, it shall do the following upon receiving the LT_Fall Transaction: 2. Transition to the Uninitialized Unplugged state.



4.4.6.2.1.2#3	NT	If the Link Partner of the disabled Adapter is the Upstream Adapter, it shall do the following upon receiving the LT_Fall Transaction: 3. Transition to the Uninitialized Plugged state as a result of detecting SBRX driven high.
4.4.6.2.1.2#4	TD 4.007	If the Link Partner of the disabled Adapter is the Upstream Adapter, it shall do the following upon receiving the LT_Fall Transaction: 4. Start lane Initialization from Phase 1.
<b>4.4.6.2.2 Enable Flow</b>		
<b>4.4.7 Time Sync Notification Ordered Set (TSNOS)</b>		
4.4.7#1	NT	When a Router receives a Time Sync Notification Ordered Set (TSNOS) it shall generate a time stamp.
4.4.7#2	NT	The Time Sync Notification Ordered Set shall have the structure in Table 4-41.
4.4.7#3	NT	SCR in the Time Sync Notification Ordered Set payload shall be set to 11 0000 1101b to indicate that the Ordered Set contents are not scrambled.
<b>4.5 Sleep and Wake</b>		
<b>4.5.1 Entry to Sleep</b>		
4.5.1#1	NT	(Host Router) A Router shall enter sleep state when the <i>Enter Sleep</i> bit is set to 1b and one of the following sleep events occur: The Router is a PCIe Host Router and it receives a PCIe PERST# signal that transitions from logical high to logical low.
4.5.1#2	CH11	If the Router tunnels PCIe traffic, then it shall send at least 3 PERST Active Tunneled Packets on each Downstream Facing Port before entering Sleep state.
4.5.1#3	NT	(Host Router) A Router shall enter sleep state when the <i>Enter Sleep</i> bit is set to 1b and one of the following sleep events occur: The Router receives an implementation-specific signal indicating entry to Sleep state.
4.5.1#4	CH11	(Device Router) A Router shall enter sleep state when the Enter Sleep bit is set to 1b and one of the following sleep events occur: The Router tunnels PCIe traffic and receives a PERST Active Tunneled Packet on the Upstream Facing Port.
4.5.1#5	NT	(Device Router) A Router shall enter sleep state when the Enter Sleep bit is set to 1b and one of the following sleep events occur: The Router receives an LT_LRoff Transaction on the Sideband Channel of an Upstream Facing Port.
4.5.1#6	NT	A Router shall not enter sleep state unless the Enter Sleep bit is set to 1b before a sleep event occurs.

4.5.1#7	NT	After the Enter Sleep bit is set to 1b, the Router shall complete any pending transactions on the Sideband Channel.
4.5.1#8	NT	When the Router is ready for the sleep event it shall set the <i>Sleep Ready</i> bit to 1b.
4.5.1#9	NT	After a sleep event occurs, the Router shall do the following for each USB4 Port: If the <i>USB4 Port is inter-Domain</i> bit is 0b and the <i>USB4 Port is Configured</i> bit is 0b, perform a disconnect by driving its SBTX line low for tDisconnectTx. If the <i>Enable Wake on Connect</i> bit of the USB4 Port is 1b, the USB4 Port shall drive its SBTX line high after tDisconnectTx.
4.5.1#10	NT	After a sleep event occurs, the Router shall do the following for each USB4 Port: If the <i>USB4 Port is inter-Domain</i> bit is 1b and the <i>Enable Wake on inter-Domain</i> bit is set to 0b, perform a disconnect by driving its SBTX line low for tDisconnectTx.
4.5.1#11	CH11	After a sleep event occurs, the Router shall do the following for each USB4 Port: Else: If the Router supports PCIe Tunneling, send at least 3 PERST Active Tunneled Packets on all Downstream PCIe Adapters that have the <i>Path Enable</i> bit set to 1b.
4.5.1#12	NT	After a sleep event occurs, the Router shall do the following for each USB4 Port: Else: Send an LT_LRoff Transaction on the Sideband Channel within tLRoffResponse from detecting the sleep event.
4.5.1#13	NT	After a sleep event occurs, the Router shall do the following for each USB4 Port: Else: If the <i>USB4 Port is Inter-Domain</i> bit is 0b and the <i>USB4 Port is Configured</i> bit is 1b, wait for an LT_LRoff Transaction on the Sideband Channel, unless an LT_LRoff Transaction was already received from the time the <i>Enter Sleep</i> bit was set to 1b.
4.5.1#14	NT	After a sleep event occurs, the Router shall do the following for each USB4 Port: Else: Transition the Adapters to CLd state.
<b>4.5.2 Behavior in Sleep State</b>		
4.5.2#1	NT	On entry to sleep state, a Router shall restore all Configuration Spaces to their default values.
4.5.2#2	NT	If the Enter Sleep bit is set to 1b, a Router shall retain a copy of the state information listed in Table 4-42 separate from Configuration Space.
4.5.2#3	NT	If a USB4 Port has the <i>USB4 Port is inter-Domain</i> state set to 1b, then the USB4 Port shall ignore any Transactions received on the Sideband Channel while in Sleep state.

4.5.3 Wake Events		
4.5.3#1	NT	A Router shall issue a Wake on Connect if the Enable Wake on Connect bit of a USB4 Port is set to 1b, the USB4 Port is Configured bit is 0b, and it detects either of the following after the Enter Sleep bit is set to 1b and it detects either of the following: A connection on the USB Type-C connector attached to the USB4 Port.
4.5.3#2	NT	A Router shall issue a Wake on Connect if the Enable Wake on Connect bit of a USB4 Port is set to 1b, and it detects either of the following: SBRX is at logic high on the USB4 Port for tConnectRx.
4.5.3#3	IOP	A Router shall issue a Wake on Disconnect event if the Enable Wake on Disconnect bit of a USB4 Port is set to 1b, the USB4 Port is Inter-Domain bit is set to 0b, the USB4 Port is Configured bit is set to 1b, and the Router detects either of the following after the Enter Sleep bit is set to 1b: A disconnect on the USB Type-C connector attached to the USB4 Port.
4.5.3#4	IOP	A Router shall issue a Wake on Disconnect event if the <i>Enable Wake on Disconnect</i> bit of a USB4 Port is set to 1b, the <i>USB4 Port is Inter-Domain</i> bit is set to 0b, the <i>USB4 Port is Configured</i> bit is set to 1b, and the Router detects either of the following after the <i>Enter Sleep</i> bit is set to 1b: SBRX is at logic low on the USB4 Port for tDisconnectRx.
4.5.3#5	IOP	A Router shall issue a Wake on Inter-Domain event if the Enable Wake on Inter-Domain bit is set to 1b, the USB4 Port is Inter-Domain bit is set to 1b, and the Router detects either of the following after the Enter Sleep bit is set to 1b: A disconnect on the USB Type-C connector attached to the USB4 Port.
4.5.3#6	IOP	A Router shall issue a Wake on Inter-Domain event if the Enable Wake on Inter-Domain bit is set to 1b, the USB4 Port is Inter-Domain bit is set to 1b, and the Router detects either of the following after the Enter Sleep bit is set to 1b: SBRX is at logic low on the USB4 Port for tDisconnectRx.
4.5.3#7	CH11	A Router shall issue a Wake on PCIe event if the Enable Wake on PCIe bit is set to 1b, and it detects a PCIe Wake event from any connected PCIe Endpoint or Switch after a Sleep Event occurs.
4.5.3#8	CH11	A Router shall issue a Wake on USB3 event if the Enable Wake on USB3 bit is set to 1b, and it detects a USB Wake event from any connected USB device after a Sleep Event occurs.
4.5.3#9	IOP	A Router shall issue a Wake on USB4 event if the USB4 Port is inter-Domain bit is set to 0b, the USB4 Port is Configured bit is set to 1b, and the Router detects at least one transition of SBRX to logical low for tWake time after a Sleep Event occurs.
4.5.3#10	TBD	A Router shall issue a Wake on DP event if the Enable Wake on DP bit is set to 1b, and it detects an HPD change or reception of an HPD IRQ after a Sleep Event occurs.

<b>4.5.4 Exit from Sleep</b>		
<b>4.5.4.1 Upstream Facing Port Disconnect</b>		
4.5.4.1#1	NT	When a Router detects a disconnect on the UFP, it shall exit sleep state
<b>4.5.4.2 Wake on USB4 Event</b>		
4.5.4.2#1	IOP	A Router shall assert SBRX to logical low for tWake time to indicate a Wake on USB4 event.
4.5.4.2#2	NT	After detecting a wake event, a Router shall: 1. issue a Wake on USB4 event on all connected USB4 Ports by asserting SBTX to logical low for tWake time.
4.5.4.2#3	NT	After detecting a wake event, a Router shall: 2. begin Lane Initialization on all connected USB4 Ports.
4.5.4.2#4	NT	The transmitting USB4 Port shall retry the Transactions as defined in Section 4.1.1.2.5.
4.5.4.2#5	NT	After detecting a wake event, the Router shall: 3. for every Adapter that reaches CL0 state, send a Hot Plug Event Packet to the Connection Manager with the UPG bit set to 0b.
<b>4.6 Timing Parameters</b>		

## Chapter 8

The following Table presents the USB4 Specification Chapter 8 asserts.

Assertion #	Test Name	Assertion Description
<b>8 Configuration Spaces</b>		
<b>8.2 Configuration Spaces</b>		
<b>8.2.2 Adapter Configuration Space</b>		
<b>8.2.2.3 Lane Adapter Configuration Capability</b>		
8.2.2.3#21	TD 4.005	The Negotiated Link Width field shall indicate the negotiated Link width (xN – corresponding to N Lanes).
<b>8.2.2.4 USB4 Port Capability</b>		
8.2.2.4#21	NT	An Adapter shall set the Router Detected bit to 1b when the USB4 Port detects a connected Router.
8.2.2.4#22	NT	An Adapter shall set the Router Detected bit to 0b upon a disconnect.
8.2.2.4#23	NT	An Adapter shall set the Wake on Connect Status bit to 1b after a wake event is generated by the USB4 Port as a result of a connect to the USB4 Port.
8.2.2.4#24	NT	The Wake on Connect Status bit shall not be set to 1b unless the Enable Wake on Connect bit is 1b.
8.2.2.4#25	NT	The Wake on Connect Status bit shall be set to 0b on entry to sleep.
8.2.2.4#26	NT	An Adapter shall set the Wake on Disconnect Status bit to 1b after a wake event is generated by the USB4 Port as a result of a disconnect from the USB4 Port.
8.2.2.4#27	NT	The Wake on Disconnect Status bit shall not be set to 1b unless the Enable Wake on Disconnect bit is 1b.
8.2.2.4#28	NT	The Wake on Disconnect Status bit shall be set to 0b on entry to sleep.
8.2.2.4#29	NT	An Adapter shall set the <i>Wake on USB4 Wake Status</i> bit to 1b after a wake event is generated by the USB4 Port as a result of a USB4 Wake.
8.2.2.4#30	NT	The <i>Wake on USB4 Wake Status</i> bit shall not be set to 1b unless the <i>Enable Wake on USB4 Wake</i> bit is 1b.
8.2.2.4#31	NT	The <i>Wake on USB4 Wake Status</i> bit shall be set to 0b on entry to sleep.
8.2.2.4#32	NT	An Adapter shall set the Wake on Inter-Domain Status bit to 1b after a wake event is generated by the USB4 Port as a result of an inter-Domain Wake.

8.2.2.4#33	NT	The Wake on Inter-Domain Status bit shall not be set to 1b unless the Enable Wake on inter-Domain bit is 1b.
8.2.2.4#34	NT	The Wake on Inter-Domain Status bit shall be set to 0b on entry to sleep.

## Chapter 13

The following Table presents the USB4 Specification Chapter 13 asserts.

Assertion #	Test Name	Assertion Description
<b>13 Interoperability with Thunderbolt™ 3 (TBT3) Systems</b>		
<b>13.2 Logical Layer</b>		
<b>13.2.1 Sideband Channel</b>		
<b>13.2.1.1 Bidirectional Re-timer</b>		
13.2.1.1#1	IOP	A Router shall implement a bidirectional Sideband Channel when attached directly to a bidirectional Cable Re-timer.
13.2.1.1#2	IOP	A Router shall implement a unidirectional Sideband Channel when not attached directly to a bidirectional Cable Re-timer.
13.2.1.1#3	IOP	A Router that is connected directly to a bidirectional Re-timer shall support concurrent reception of Transactions on SBTX and on SBRX.
13.2.1.1#4	NT	A Router shall drive its SBTX for up to 2 bit times after the last Stop bit of an AT Command.
<b>13.2.1.2 Transactions</b>		
<b>13.2.1.2.1 LT Transactions</b>		
13.2.1.2.1#1	IOP	A Router shall support the additional LT Transaction types defined in Table 13-2.
<b>13.2.1.2.2 AT Transactions</b>		
13.2.1.2.2#1	BC	The structure of the STX Symbol within an AT Transaction shall be as defined in Table 13-3.
13.2.1.2.2#2	NT	Bit 4 in the STX symbol (Responder) shall be set to 1b by a Re-timer in an AT Response when operating in an active cable with bidirectional Re-timers.
13.2.1.2.2#3	BC	Bit 4 in the STX symbol (Responder) shall be set to 0b in all other cases.
13.2.1.2.2#4	NT	Bit 2 in the STX symbol (Recipient): For an AT Command: shall be 0b if a Cable Re-timer is the intended final recipient or 1b if a Router is the intended final recipient
13.2.1.2.2#5	BC	Bit 2 in the STX symbol (Recipient): For an AT Response: shall be set to 1b

13.2.1.2.2#6	NT	A Router shall not send an AT Command that targets Register 13 of a Re-timer or Router SB Register Space unless the Re-timer or Router is directly attached to it.
<b>13.2.1.2.2.1 Bounce Mechanism</b>		
13.2.1.2.2.1#1	TD 13.1.001	A Router shall support the Bounce Mechanism.
13.2.1.2.2.1#2	TD 13.1.001	A Router shall set the Bounce bit to 1b and the ReturnBounce bit to 1b to target a Cable Re-timer that is adjacent to the Router's Link Partner.
13.2.1.2.2.1#3	TD 13.1.001	A Router that receives an AT Transaction with the Bounce bit set to 1b and the ReturnBounce bit to 1b shall set the Bounce bit to 0b, then forward the AT Transaction towards its adjacent Cable Re-timer.
13.2.1.2.2.1#4	TD 13.1.001	A Router that receives an AT Response with the Bounce bit set to 1b and the ReturnBounce bit to 0b shall set the Bounce bit to 0b, then forward the AT Response to its Link Partner.
<b>13.2.1.2.3 RT Transactions</b>		
13.2.1.2.3#1	BC	Byte 2 in a Broadcast RT Transaction shall have the format in Table 4-7 with the changes in Table 13-4.
<b>13.2.1.3 SB Register Space</b>		
13.2.1.3#1	TD 13.1.002	A Router shall support the additional registers and register fields in Table 13-5 and Table 13-6.
<b>13.2.1.4 Lane Initialization</b>		
<b>13.2.1.4.1 Phase 1 – Determination of Initial Conditions</b>		
13.2.1.4.1#1	IOP	A Router shall not continue on to Phase 2 until it has obtained the connection information described in this section and in Section 4.1.2.1.
13.2.1.4.1#2	IOP	If TBT3 Mode is established on the Link, a Router shall proceed with Lane Initialization as defined in Section 4.1.2 with the changes defined in this chapter.
<b>13.2.1.4.2 Phase 3 – Determination of USB4 Port Characteristics</b>		
13.2.1.4.2#1	IOP	Router shall decide the Lane attributes using the decision criteria in Table 4-18 with the changes defined in Table 13-7.
13.2.1.4.2#2	IOP	Router A shall enable RS-FEC if at least one side of the Link requests it (i.e. the RS-FEC Request (Gen 2) bit is set to 1b in the SB Register Space of the local USB4 Port and/or its Link Partner).
13.2.1.4.2#3	IOP	Otherwise, RS-FEC shall not be enabled.



13.2.1.4.2#4	IOP	Router A shall set the RS-FEC Enabled (Gen 2) bit in the USB4 Port Capability to reflect whether it is operating with RS-FEC.
13.2.1.4.2#5	TD 13.1.003	The Sideband Channel of Router A shall operate as a USB4 Sideband Channel if all of the following are true: The USB4 Sideband Channel Support bit in the SB Register Space of both Routers is 1b; The Link is over either a Passive Cable or an Active Cable with unidirectional Re-timers.
13.2.1.4.2#6	TD 13.1.003	Else, the Sideband Channel of Router A shall operate as a TBT3-Compatible Sideband Channel.
13.2.1.4.2#7	TD 13.1.003	When sending a Broadcast RT Transaction on a USB4 Sideband Channel, Router A shall set the USB4 bit to 1b.
13.2.1.4.2#8	TD 13.1.003	When sending a Broadcast RT Transaction on a TBT3-Compatible Sideband Channel, Router A shall set the USB4 bit to 0b.
<b>13.2.1.4.3 Phase 4 – Lane Parameters Synchronization and Transmit Start</b>		
13.2.1.4.3#1	TD 13.1.003	Router A shall do the following for each enabled Lane to indicate that it is ready to start transmission on a given Lane:
13.2.1.4.3#2	TD 13.1.003	If the Router Assembly for Router A does not include any On-Board Re-timers, and if operating at Gen 2 speed, Router A shall send an LT_Gen_2 Transaction for each enabled Lane every tLaneParams.
13.2.1.4.3#3	TD 13.1.003	Router A shall continue sending LT_Gen_2 Transactions until all of the following are true, then continue to Step 2: At least tLTPhase4 time has passed from completion of Phase 2; Router A has sent LT_Gen_2 Transactions at least twice; Router A has received an LT_Gen_2 Transaction from Router B.
13.2.1.4.3#4	TD 13.1.003	If the Router Assembly for Router A does not include any On-Board Re-timers, and if operating at Gen 3 speed, Router A shall send an LT_Gen_3 Transaction for each enabled Lane every tLaneParams.
13.2.1.4.3#5	TD 13.1.003	Router A shall continue sending LT_Gen_3 Transactions until all of the following are true, then continue to Step 2: At least tLTPhase4 time has passed from completion of Phase 2; Router A has sent LT_Gen_3 Transactions at least twice; Router A has received an LT_Gen_3 Transaction from Router B.
13.2.1.4.3#6	TD 13.1.003	If the Router Assembly for Router A includes one or more On-Board Re-timers, and if operating at Gen 2 speed, Router A shall send a Broadcast RT Transaction every tLaneParams.
13.2.1.4.3#7	TD 13.1.003	The Broadcast RT Transaction shall have the parameter values in Table 4-18.
13.2.1.4.3#8	TD 13.1.003	Router A shall also send an LT_Gen_2 Transaction for each enabled Lane.

13.2.1.4.3#9	TD 13.1.003	Router A shall continue sending the Broadcast RT and LT_Gen_2 Transactions until all of the following conditions are true: At least tLTPHase4 time has passed from completion of Phase 2; Router A has sent LT_Gen_2 Transactions at least twice; Router A has received an LT_Gen_2 Transaction from Router B.
13.2.1.4.3#10	TD 13.1.003	If the Router Assembly for Router A includes one or more On-Board Re-timers, and if operating at Gen 3 speed, Router A shall send a Broadcast RT Transaction every tLaneParams.
13.2.1.4.3#11	TD 13.1.003	The Broadcast RT Transaction shall have the parameter values in Table 4-18.
13.2.1.4.3#12	TD 13.1.003	Router A shall also send an LT_Gen_3 Transaction for each enabled Lane.
13.2.1.4.3#13	TD 13.1.003	Router A shall continue sending the Transactions until all of the following conditions are true: At least tLTPHase4 time has passed from completion of Phase 2; Router A has sent LT_Gen_3 Transactions at least twice; Router A has received an LT_Gen_3 Transaction from Router B.
<b>13.2.1.4.4 Phase 5 – Link Equalization</b>		
13.2.1.4.4#1	TD 13.1.003	(Transmitter) If Router A connects to an On-Board Re-timer in the same Router Assembly, then Router A's transmitter shall perform the transmitter flow in the symmetric equalization flow defined in Section 4.1.2.5.1.
13.2.1.4.4#2	TD 13.1.003	(Transmitter) If Router A connects to a Cable Re-timer: Router A's transmitter shall perform the Primary Partner flow in the Asymmetric TxFFE Parameter Negotiation with a transmitting Primary Partner defined in Section 13.2.1.4.4.1.
13.2.1.4.4#3	TD 13.1.003	(Transmitter) If Router A connects to a Cable Re-timer: Once a transmitter completes TxFFE negotiation with the Cable Re-timer's receiver, Router A shall send an LT_Resume2 Transaction on the USB4 Port that completed negotiation with the LSELane field matching the Lane number that completed negotiation.
13.2.1.4.4#4	TD 13.1.003	(Transmitter) If Router A either connects directly to Router B or connects to an On-Board Re-timer in the Router Assembly of Router B (through a Passive Cable or Cable with re-driver), then Router A's transmitter shall perform the transmitter flow in the symmetric equalization flow defined in Section 4.1.2.5.1.
13.2.1.4.4#5	TD 13.1.003	(Receiver) If Router B connects to an On-Board Re-timer, then Router B's receiver shall perform the receiver flow in the symmetric equalization flow defined in Section 4.1.2.5.1.
13.2.1.4.4#6	TD 13.1.003	(Receiver) When a receiver's equalization flow is complete on a Lane, the Router shall set the Lane's Clock Switch Done bit to 1b
13.2.1.4.4#7	TD 13.1.003	(Receiver) If Router B connects to a Cable Re-timer, then Router B's receiver shall perform the Primary Partner flow in the Asymmetric TxFFE Parameter Negotiation with a Receiving Primary Partner defined in Section 13.2.1.4.4.2.

13.2.1.4.4#8	TD 13.1.003	(Receiver) If Router B either connects directly to Router A or connects to an On-Board Re-timer in the Router Assembly of Router A, then Router B's receiver shall perform the receiver flow in the symmetric equalization flow defined in Section 4.1.2.5.1.
<b>13.2.1.4.4.1 Phase 5 – Asymmetric TxFFE Parameter Negotiation with a Transmitting Primary Partner</b>		
<b>Transmitting Primary Partner flow:</b>		
13.2.1.4.4.1#1	TD 13.1.003	1) The transmitter shall start with the TX Active bit set to 1b (default value) in the Tx Status byte of the TxFFE register
13.2.1.4.4.1#2	TD 13.1.003	2) The transmitter shall send an AT Transaction with a write Command to the receiver that sets the Tx Active bit to 1b in the Partner Tx Status byte in the TxFFE register
13.2.1.4.4.1#3	TD 13.1.003	3) The transmitter shall read the local <i>Rx Status &amp; TxFFE Request</i> byte from the receiver.
13.2.1.4.4.1#4	TD 13.1.003	4) On reception of an AT Response from the receiver, the transmitter shall copy the transaction contents into its <i>Rx Status &amp; TxFFE Request</i> byte.
13.2.1.4.4.1#5	TD 13.1.003	4) If Rx Locked = 1b, then negotiation is complete and no further TxFFE negotiation steps shall be taken.
13.2.1.4.4.1#6	TD 13.1.003	4) Else if New Request = 0b and TxFFE Request is the same as the previous TxFFE Request, the receiver has not provided a new request yet. The Router shall go to Step 3. The Router shall perform Step 3 within tPollTXFFE of receiving the AT Response.
13.2.1.4.4.1#7	TD 13.1.003	4) Else, this is a new request to update TxFFE parameters. Continue on to Step 5.
13.2.1.4.4.1#8	TD 13.1.003	5) The transmitter shall update its transmitter parameters based on the new parameters received in the AT Response
13.2.1.4.4.1#9	TD 13.1.003	5) If both Lane Adapters in the Port are enabled and have not yet completed TxFFE negotiation, both transmitters must complete Step 5 before continuing to Step 6. If the other Lane Adapter has not yet completed Step 5, the transmitter shall wait for the other Lane to finish Step 5 before continuing to Step 6.
13.2.1.4.4.1#10	TD 13.1.003	6) The transmitter shall inform the receiver that it has updated to new parameters by sending an AT Transaction with a write Command to the receiver targeting its Partner Tx Status byte in the TxFFE register with the following contents: Tx Active = 1b; TxFFE Setting = value received in Step 4.
13.2.1.4.4.1#11	TD 13.1.003	7) The transmitter shall read the local <i>Rx Status &amp; TxFFE Request</i> byte from the receiver.

13.2.1.4.4.1#12	TD 13.1.003	8) On reception of an AT Response from the receiver, the transmitter shall copy the transaction contents into its <i>Rx Status &amp; TxFFE Request</i> byte
13.2.1.4.4.1#13	TD 13.1.003	8) If New Request = 1b and TxFFE Request is the same as the previous TxFFE Request, the Router shall return to and perform Step 7 within tPollTXFFE of receiving the AT Response.
13.2.1.4.4.1#14	TD 13.1.003	8) Else, go to Step 3.
<b>13.2.1.4.4.2 Phase 5 – Asymmetric TxFFE Parameter Negotiation with a Receiving Primary Partner</b>		
<b>Receiving Primary Partner flow:</b>		
13.2.1.4.4.2#1	TD 13.1.003	1) The receiver shall start with the following default values in the <i>Rx Status &amp; TxFFE Request</i> byte of the TxFFE register: Rx Locked = 0b; New Request bit = 0b; Rx Active bit = 0b.
13.2.1.4.4.2#2	TD 13.1.003	2) The receiver shall read the Local Tx Status byte of the transmitter.
13.2.1.4.4.2#3	TD 13.1.003	2) On reception of an AT Response from the transmitter, the receiver shall do the following: If Tx Active = 1b (i.e. the transmitter is transmitting), then enable the receiver, set Rx Active to 1b, and go to Step 3. Else, repeat Step 2 within tPollTXFFE of receiving the AT Response.
13.2.1.4.4.2#4	TD 13.1.003	3) The receiver shall evaluate its receiver behavior. If equalization is complete, the receiver shall set the Rx Locked field to 1b.
13.2.1.4.4.2#5	TD 13.1.003	4) The receiver shall do the following: If Rx Locked = 1, then go to Step 5. Else, go to Step 6
13.2.1.4.4.2#6	TD 13.1.003	5) TXFFE negotiation is complete.
13.2.1.4.4.2#7	TD 13.1.003	6) The receiver shall select a new set of TxFFE parameters.
13.2.1.4.4.2#8	TD 13.1.003	7) The receiver shall write the Partner <i>Rx Status &amp; TxFFE Request</i> byte at the transmitter as follows: If the Transmitting Primary Partner finished TxFFE on both Lanes, then the receiver sends an AT Command with a write Command targeting the Partner <i>Rx Status &amp; TxFFE Request</i> byte of the TxFFE register of the transmitter. Else, the receiver will wait for the next AT Command with a write Command to the TxFFE Register from the Transmitting Primary Partner and use it to write the Partner <i>Rx Status &amp; TxFFE Request</i> byte of the TxFFE register of the transmitter. The AT command shall write to following values to the following fields: New Request = 1b; Rx Active = 1b; TxFFE Request = index of selected set of TxFFE parameters.
13.2.1.4.4.2#9	TD 13.1.003	8) The receiver shall wait for a write Response indicating the transmitter is using the new requested TxFFE settings.
13.2.1.4.4.2#10	TD 13.1.003	9) The receiver shall evaluate its receiver behavior. If equalization is complete, the receiver shall set the Rx Locked field to 1b.

13.2.1.4.4.2#11	TD 13.1.003	10) The receiver shall write the Partner <i>Rx Status &amp; TxFFE Request</i> byte at the transmitter as follows: If the Transmitting Primary Partner finished TxFFE on both Lanes, then the receiver sends an AT Command with a write Command targeting the Partner <i>Rx Status &amp; TxFFE Request</i> byte of the TxFFE register of the transmitter.
13.2.1.4.4.2#12	TD 13.1.003	10) The receiver shall write the Partner <i>Rx Status &amp; TxFFE Request</i> byte at the transmitter as follows: Else, the receiver will wait for the next AT Command with a write Command to the TxFFE Register from the Transmitting Primary Partner and use it to write the Partner <i>Rx Status &amp; TxFFE Request</i> byte of the TxFFE register of the transmitter. The AT Command shall write to following values to the following fields: New Request = 0b; Rx Active = 1b; Rx Locked = updated value
13.2.1.4.4.2#13	TD 13.1.003	11) The receiver shall do the following: If Rx Locked = 1, then go to Step 5. Else, go to Step 6.
<b>13.2.2 Logical Layer State Machine</b>		
<b>13.2.2.1 CLd State</b>		
<b>13.2.2.1.1 Behavior in State</b>		
13.2.2.1.1#1	NT	A USB4 Port that is TBT3-Compatible shall support the behavior defined in this section in addition to the behavior described in Section 4.2.1.2.2.
13.2.2.1.1#2	NT	A Lane Adapter (that is not the Upstream Adapter) that enters this state due to reception of an LT_Fall Transaction shall start Lane Initialization when it receives a Broadcast RT Transaction, an LT_Gen_2 Transaction, or an LT_Gen_3 Transaction.
13.2.2.1.1#3	NT	A Lane 0 Adapter shall not start Lane Initialization until it receives one of the following: A Broadcast RT Transaction with the Lane0Enabled bit set to 1b; An LT_Gen_2 Transaction with the LSELane bit set to 0b; An LT_Gen_3 Transaction with the LSELane bit set to 0b.
13.2.2.1.1#4	NT	A Lane 1 Adapter shall not start Lane Initialization until it receives one of the following: A Broadcast RT Transaction with the Lane1Enabled bit set to 1b; An LT_Gen_2 Transaction with the LSELane bit set to 1b; An LT_Gen_3 Transaction with the LSELane bit set to 1b.
13.2.2.1.1#5	NT	The Lane Adapter shall start Lane Initialization from Phase 4.
13.2.2.1.1#6	NT	The Lane Adapter shall maintain any state acquired in Phases 1 through 3 of previous Lane Initialization.
<b>13.2.2.2 TS1 and TS2 Ordered Sets</b>		
13.2.2.2#1	IOP	When operating in TBT3 mode, TS1 and TS2 Ordered Sets shall have the format shown in Table 4-25 with the changes in Table 13-8.

13.2.2.2#2	IOP	Lane Bonding Target 2. Transmitter shall either set this value to match the Lane Bonding Target field or shall set this value to 001b.
13.2.2.2#3	NT	Lane Bonding Target 2. A Receiver shall ignore this field.
<b>13.2.3 USB4 Link Operation</b>		
<b>13.2.3.1 USB4 Link Transitions</b>		
13.2.3.1#1	IOP	When TBT3 Mode is established on the Link, a USB4 Port shall support the transitions described in Section 4.2.2 with the following changes:
13.2.3.1#2	TD 13.1.004	For a Device Router that supports TBT3 Mode on its Upstream Facing Port, all USB4 Ports shall support operation with two independent Single-Lane Links.
<b>13.2.3.2 Pre-Coding</b>		
13.2.3.2#1	NT	In addition to the conditions defined in Section 4.3.6.2, Pre-Coding shall be off when the Link uses a TBT3-Compatible Sideband Channel.
<b>13.2.4 Sleep and Wake</b>		
13.2.4#1	NT	If bits 15:12 in the Connection Manager USB4 Version field in the Router Configuration Space are 0b (indicating a TBT3 Connection Manager), a Router shall support Sleep and Wake per Section 4.5 with the changes defined in this section.
<b>13.2.4.1 Entry to Sleep</b>		
13.2.4.1#1	NT	After the Enter Sleep bit is set to 1b in all Ports, a Device Router shall do the following for each USB4 Port: Transition the USB4 Adapters to CLd state.
13.2.4.1#2	NT	After the Enter Sleep bit is set to 1b in all Ports, a Device Router shall do the following for each USB4 Port: If any of the following conditions apply, the USB4 Port shall go through disconnect: For Lane 0 in a USB4 Port: The Lane 0 is Inter-Domain bit is 0b and the Lane 0 Configured bit is 0b; The Lane 0 is Inter-Domain bit is 1b and the Inter-Domain Disconnect on Sleep bit is set to 1b.
13.2.4.1#3	NT	After the Enter Sleep bit is set to 1b in all Ports, a Device Router shall do the following for each USB4 Port: If any of the following conditions apply, the USB4 Port shall go through disconnect: For Lane 1 in a USB4 Port: The Lane 1 is Inter-Domain bit is 0b and the Lane 1 Configured bit is 0b; The Lane 1 is Inter-Domain bit is 1b and the Inter-Domain Disconnect on Sleep bit is set to 1b.
<b>13.2.4.2 Behavior in Sleep State</b>		
13.2.4.2#1	NT	A Device Router shall retain a copy of the state information listed in Table 13-9 separate from Configuration Space.

13.2.4.2#2	NT	If Lane 0 of a USB4 Port is disconnected while in Sleep state, then the internal Lane 0 is Inter-Domain state and Lane 0 Configured state listed in Table 13-9 shall both transition to 0b.
13.2.4.2#3	NT	If Lane 1 of a USB4 Port is disconnected while in Sleep state, then the internal Lane 1 is Inter-Domain state and Lane1 Configured state listed in Table 13-9 shall both transition to 0b.
<b>13.2.4.3 Wake Events</b>		
13.2.4.3#1	NT	A Device Router shall support all of the wake events listed in the Enable Wake Events field of the USB4 Port Region in the Vendor Specific Extended 6 Capability of the Router Configuration Space.
<b>13.2.4.4 Exit From Sleep</b>		
13.2.4.4#1	NT	A Device Router shall not start Lane Initialization for Lane 0 until the Start Link Initialization bit is set to 1b, if either of the following is true on exit from sleep: The Lane 0 Configured state is set to 0b; The Lane 0 is Inter-Domain bit is 1b.
13.2.4.4#2	NT	A Device Router shall not start Lane Initialization for Lane 1 until the Start Link Initialization bit is set to 1b, if either of the following is true on exit from sleep: The Lane 1 Configured state is set to 0b; The Lane 1 is Inter-Domain bit is 1b.
<b>13.2.5 Timing Parameters</b>		

## Re-timer Assertions

### Chapter 4

The following Table presents the USB4 Re-timer Specification Chapter 4 asserts.

Assertion #	Test Name	Assertion Description
<b>4. Logical Layer</b>		
4#1rt	NT	A Re-timer shall have two USB4 Ports.
4#2rt	NT	The USB4 Ports on a Re-timer shall have the same number of Lane Adapters and shall support the same capabilities.
<b>4.1 Sideband Channel</b>		
<b>4.1.1 Transactions</b>		
4.1.1#1rt	IOP	When forwarding Transactions from an SBRX input to an SBTX output, a Re-timer shall maintain the order of Transactions as received on the SBRX input.
<b>4.1.1.1 LT Transactions</b>		
4.1.1.1#1rt	IOP	A Re-timer shall support LT Transactions as defined in the USB4 Base Specification with the following changes:
4.1.1.1#2rt	IOP	When a Re-timer receives an LT Transaction, it shall forward the Transaction to its other USB4 Port.
<b>4.1.1.2 AT Transactions</b>		
4.1.1.2#1rt	NT	A Re-timer shall support AT Transactions as defined in the USB4 Base Specification with the following changes:
4.1.1.2#2rt	NT	A Cable Re-timer shall forward an AT Transaction, regardless of the value of the Recipient bit.
4.1.1.2#3rt	NT	An On-Board Re-timer shall forward an AT Transaction, regardless of the value of the Recipient bit.
4.1.1.2#4rt	NT	A Re-timer shall not initiate AT Commands.
<b>4.1.1.3 RT Transactions</b>		
4.1.1.3#1rt	NT	A Re-timer shall support RT Transactions as defined in the USB4 Base Specification with the changes defined in this section.



<b>4.1.1.3.1 Broadcast RT Transaction</b>		
4.1.1.3.1#1rt	BC TD 4.005	When a Re-timer receives a Broadcast RT Transaction on its Router-Facing USB4 Port, it shall increment the value in the Index field of the Transaction by one and shall store the resulting Re-timer Index locally as its Router-Facing Index.
4.1.1.3.1#2rt	TD 4.005	The Re-timer shall then forward the Broadcast RT Transaction.
4.1.1.3.1#3rt	NT	When a Re-timer receives a Broadcast RT Transaction on its Cable-Facing USB4 Port, it shall increment the value in the Index field of the Transaction by one and shall store the resulting Re-timer Index locally as its Cable-Facing Index.
4.1.1.3.1#4rt	NT	The Re-timer shall then forward the Broadcast RT Transaction.
4.1.1.3.1#5rt	TD 4.005	When a Re-timer forwards a Broadcast Transaction, it shall set the SSCalways bit to 0b to indicate that the Re-timer supports exiting CLx state with SSC turned off.
<b>4.1.1.3.2 Addressed RT Transaction</b>		
4.1.1.3.2#1rt	NT	When sending an Addressed RT Command, a Re-timer shall set the Index field to 0.
4.1.1.3.2#2rt	IOP	When a Re-timer receives an Addressed RT Command with the Index field set to 0, it shall process the Command and send a response as described in the USB4 Base Specification. The Re-timer shall not forward the Transaction.
4.1.1.3.2#3rt	NT	When a Re-timer receives an Addressed RT Command on its Router-Facing USB4 Port with an Index field that matches its Router-Facing Index, it shall process the Command and send a response as described in the USB4 Base Specification. The Re-timer shall not forward the Transaction.
4.1.1.3.2#4rt	NT	When an On-Board Re-timer receives an Addressed RT Command on its Cable-Facing USB4 Port with an Index field that matches its Cable-Facing Index, it may process the Command and send a response as described in Section 4.1.2.5.1 of the USB4 Specification, but is not required to do so. It shall not forward the Command.
4.1.1.3.2#5rt	NT	When a Cable Re-timer receives an Addressed RT Command on its Cable-Facing USB4 Port with an Index field that matches its Cable-Facing Index, it shall process the Command and send a response as described in the USB4 Base Specification. The Re-timer shall not forward the Transaction.
4.1.1.3.2#6rt	NT	When a Re-timer receives an Addressed RT Transaction on its Router-Facing USB4 Port with an Index field that does not match its Router-Facing Index, it shall forward the RT Transaction without sending a response.

4.1.1.3.2#7rt	TD 4.001	When a Re-timer receives an Addressed RT Transaction on its Cable-Facing USB4 Port with an Index field that does not match its Cable-Facing Index, it shall forward the RT Transaction without sending a response.
4.1.1.3.2#8rt	IOP	If the Index field in the Addressed RT Transaction is 0, then the Re-timer shall consume the Addressed RT Response.
4.1.1.3.2#9rt	IOP	If the Index field in the Addressed RT Transaction is not 0, the Re-timer shall forward the Addressed RT Response.
<b>4.1.1.4 SB Register Space</b>		
4.1.1.4#1rt	IOP	A Re-timer shall maintain the SB Register Space defined in Table 4-1.
4.1.1.4#2rt	NT	Read Only. An AT Write Command or an RT Write Command to a field with this access type shall have no effect. An AT Read Command or an RT Read Command shall return a meaningful value
4.1.1.4#3rt	NT	Read/Write. A field with this access type shall be capable of both Read Commands and Write Commands. The value read from this field shall reflect the last value written to it unless the field was reset in the interim.
4.1.1.4#4rt	NT	Reserved. Reserved for future implementation. A Write Command to this field shall have no effect.
4.1.1.4#5rt	NT	Reserved with Non-Zero Value. Reserved for future implementation. A Write Command to this field shall have no effect. A read shall return the specified value.
4.1.1.4#6rt	IOP	The SB Register Space registers shall have the structure and fields described in Table 4-3.
<b>4.1.2 Lane Initialization</b>		
4.1.2#1rt	NT	A Re-timer shall perform Lane Initialization as described in the USB4 Base specification with the modifications described in this section.
<b>4.1.2.1 Phase 1 - Determination of Initial Conditions</b>		
4.1.2.1#1rt	IOP	An On-Board Re-timer shall also determine whether or not there is a reverse insertion at the USB Type-C connector.
4.1.2.1#2rt	NT	A Re-timer shall not continue on to Phase 2 until it has obtained the connection information listed above.
4.1.2.1#3rt	NT	A Re-timer shall not proceed to phase 2 unless USB4 Mode is established on the Link.
<b>4.1.2.1.1 Lane Reversal</b>		
4.1.2.1.1#1rt	IOP	When necessary to correct for Lane mismatch, Lane reversal shall take place in phase 1.

4.1.2.1.1#2rt	IOP	An On-Board Re-timer that is adjacent to the USB Type-C connector shall swap its SBTX and SBRX lines facing the connector.
4.1.2.1.1#3rt	IOP	An On-Board Re-timer shall swap its designation of Lane 0 and Lane 1 in both USB4 Ports.
<b>4.1.2.2 Phase 2 - Router Detection</b>		
4.1.2.2#1rt	TD 4.005	When a Re-timer detects a logic high on SBRX of one USB4 Port for tConnectRx time, it shall drive SBTX on the other USB4 Port to logic high.
4.1.2.2#2rt	IOP	The Re-timer shall then begin forwarding Transactions on the Sideband Channel in this direction.
4.1.2.2#3rt	IOP	After both USB4 Ports detect a logic high on SBRX and drive SBTX high, the Re-timer shall transition to phase 4 of Lane Initialization.
<b>4.1.2.3 Phase 3 - Determination of USB4 Port Characteristics</b>		
<b>4.1.2.4 Phase 4 - Lane Parameters Synchronization</b>		
4.1.2.4#1rt	IOP	When a Re-timer receives a Broadcast RT Transaction it shall update its Link parameters to match the Link parameters in the Transaction.
4.1.2.4#2rt	IOP	When a Re-timer detects an LT_Resume Transaction on any USB4 Port, it shall transition to phase 5.
<b>4.1.2.5 Phase 5 - Lane Equalization</b>		
4.1.2.5#1rt	NT	Upon entry to phase 5, a receiver shall perform the receiver flow for symmetric TxFFE negotiation as defined in the USB4 Base Specification.
4.1.2.5#2rt	TD 4.005	The Re-timer shall use RT Transactions (with the Index field set to 0b) to access the SB Register Space of the adjacent USB4 Port.
4.1.2.5#3rt	NT	When the Rx Active bit for a receiver is set to 1b, the Re-timer shall turn on the Corresponding Transmitter and shall start transmitting CL_WAKE1.X Ordered Set Symbols, where X is the Re-timer Index assigned by the Router that is the target of the CL_WAKE1.X Ordered Set Symbols.
4.1.2.5#4rt	NT	The transmitter shall use a locally generated, non-SSC clock to transmit the CL_WAKE1.X Ordered Set Symbols.
4.1.2.5#5rt	NT	The Corresponding Transmitter shall then perform the transmitter flow for symmetric TxFFE negotiation as defined in the USB4 Base Specification.
4.1.2.5#6rt	NT	The Re-timer shall use Addressed RT Transactions (with the Index field set to 0b) to access the SB Register Space of the adjacent USB4 Port.

4.1.2.5#7rt	TD 4.005	A transmitter shall stop using the local clock and shall start using the recovered clock from the Corresponding Receiver when all of the following are true: The Re-timer has completed TxFFE negotiation for all transmitters in that USB4 Port and all their Corresponding Receivers; and The Clock Switch Done bit for Lane 0 of the adjacent USB4 Port is 1b.
4.1.2.5#8rt	TD 4.005	After a transmitter switches to using the receiver clock, it shall forward the bit stream it receives from the Corresponding Receiver instead of transmitting its locally-generated CL_WAKE1.X Ordered Set Symbols.
4.1.2.5#9rt	TD 4.005	The Re-timer shall set the Clock Switch Done bit in the Corresponding Receiver to 1b.
4.1.2.5#10rt	NT	During the transition from local clock to receiver clock, the Re-timer shall meet the SSC_SLEW_RATE requirement as specified in the USB4 Base Specification. The transition may or may not take place on Symbol boundary.
<b>4.2 Re-timer Channel State Machine</b>		
4.2#1rt	NT	A Re-timer Channel shall support the following states: CLd state, Bit Lock state, Forwarding state, CL0s, CL1, CL2 states.
<b>4.2.1 CLd</b>		
<b>4.2.1.1 Entry to State</b>		
4.2.1.1#1rt	NT	A Re-timer Channel shall transition to the CLd state when any of the following occur: The Re-timer is first powered on.
4.2.1.1#2rt	NT	A Re-timer Channel shall transition to the CLd state when any of the following occur: The Re-timer detects a disconnect event (i.e. SBRX transitions to logical low on any USB4 Port for more than tDisconnectRx time).
4.2.1.1#3rt	NT	A Re-timer Channel shall transition to the CLd state when any of the following occur: The SBRX of both Re-timer USB4 Ports are at logical high and both USB4 Ports receive an LT_LRoff Transaction within tLROff of each other.
4.2.1.1#4rt	NT	A Re-timer Channel shall transition to the CLd state when any of the following occur: The Re-timer Channels for Lane 0 shall also transition to CLd state when the Re-timer receives an LT_Fall Transaction on any USB4 Port with LSELane field set to 0b.
4.2.1.1#5rt	NT	A Re-timer Channel shall transition to the CLd state when any of the following occur: The Re-timer Channels for Lane 1 shall also transition to CLd state when the Re-timer receives an LT_Fall Transaction on any USB4 Port with LSELane field set to 1b.
4.2.1.1#6rt	NT	A Re-timer Channel that transitions to CLd state due to an LT_Fall Transaction shall maintain any Lane state acquired in phase 1 and phase 2 of the previous Lane Initialization.

<b>4.2.1.2 Behavior in State</b>		
4.2.1.2#1rt	NT	The Re-timer Channels for Lane 0 shall start Lane Initialization when the Re-timer receives a Broadcast RT Transaction on any USB4 Port with the Lane0 Enabled bit set to 1b.
4.2.1.2#2rt	NT	The Re-timer Channels for Lane 1 shall start Lane Initialization when the Re-timer receives a Broadcast RT Transaction on any USB4 Port with the Lane1 Enabled bit set to 1b.
<b>4.2.1.3 Exit from State</b>		
4.2.1.3#1rt	NT	A Re-timer Channel shall exit this state when its transmitter is transmitting and its receiver is enabled.
4.2.1.3#2rt	NT	After exiting the CLd state, a Re-timer Channel shall transition to the Bit Lock state.
<b>4.2.2 Bit Lock</b>		
<b>4.2.2.1 Entry to State</b>		
4.2.2.1#1rt	NT	A Re-timer Channel shall enter this state when it exits the CLd state.
<b>4.2.2.2 Behavior in State</b>		
<b>4.2.2.3 Exit from State</b>		
4.2.2.3#1rt	NT	A Re-timer Channel shall exit this state after its receiver achieves bit lock and its transmitter is transmitting the bit stream received by its receiver.
4.2.2.3#2rt	NT	After exiting the Bit Lock state, a Re-timer Channel shall transition to the Forwarding state.
<b>4.2.3 Forwarding</b>		
<b>4.2.3.1 Entry to State</b>		
4.2.3.1#1rt	NT	A Re-timer Channel shall enter this state upon successful completion of receiver lock.
<b>4.2.3.2 Behavior in State</b>		
4.2.3.2#1rt	NT	When a Re-timer Channel is in Forwarding state, it shall forward traffic from its receiver to its transmitter.
4.2.3.2#2rt	NT	A Re-timer shall forward traffic regardless of whether or not it receives Logical Layer Symbols.

4.2.3.2#3rt	NT	A Re-timer Channel shall not modify the logical level of a bit. A Re-timer Channel shall neither add nor discard any bits.
<b>4.2.3.3 Exit from State</b>		
4.2.3.3#1rt	NT	A Re-timer Channel shall only exit this state after one of the following occurs: Transition to CLd state.
4.2.3.3#2rt	NT	A Re-timer Channel shall only exit this state after one of the following occurs: Transition to CL0s, CL1, or CL2 states.
<b>4.2.4 Low Power (CL0s, CL1, and CL2)</b>		
<b>4.2.4.1 Entry to State</b>		
4.2.4.1#1rt	NT	On detection of 3 back-to-back CL2_ACK Ordered Sets, the Re-timer Lane Adapter shall start counting time in Symbol Time units.
4.2.4.1#2rt	NT	The initial value of CL2_ACK Counter shall be the number of CL2_ACK Ordered Set Symbols that were already forwarded.
4.2.4.1#3rt	NT	On detection of 3 back-to-back CL1_ACK Ordered Sets, the Re-timer Lane Adapter shall start counting time in Symbol Time units.
4.2.4.1#4rt	NT	The initial value of CL1_ACK Counter shall be the number of CL1_ACK Ordered Set Symbols that were already forwarded.
4.2.4.1#5rt	NT	While the receiver is shut down and the Channel still in Forwarding state, the transmitter shall transmit a DC balanced signal and may use a local clock without SSC.
4.2.4.1#6rt	NT	When the CL2_ACK Counter reaches a count of tEnterCLx, the Re-timer Lane Adapter shall: Transition the Re-timer Channel in the direction forwarding the CL2_ACK Ordered Sets to a CL2 state.
4.2.4.1#7rt	NT	When the CL2_ACK Counter reaches a count of tEnterCLx, the Re-timer Lane Adapter shall: Reset the CL2_ACK Counter.
4.2.4.1#8rt	NT	When the CL2_ACK Counter reaches a count of tEnterCLx, the Re-timer Lane Adapter shall: Transition the Re-timer Channel transmitter to electrical idle within tTxOff time from expiration of the CL2_ACK Counter.
4.2.4.1#9rt	NT	When the CL2_ACK Counter reaches a count of tEnterCLx, the Re-timer Lane Adapter shall: Wait tEnterLFPS1, then enable detection of Low Frequency Periodic Signaling (LFPS).
4.2.4.1#10rt	NT	While the receiver is shut down and the Channel still in Forwarding state, the transmitter shall transmit a DC balanced signal and may use local clock without SSC.

4.2.4.1#11rt	NT	When the CL1_ACK Counter reaches a count of tEnterCLx, the Re-timer Lane Adapter shall: Transition the Re-timer Channel in the direction forwarding the CL1_ACK Ordered Sets to a CL1 state.
4.2.4.1#12rt	NT	When the CL1_ACK Counter reaches a count of tEnterCLx, the Re-timer Lane Adapter shall: Reset the CL1_ACK Counter.
4.2.4.1#13rt	NT	When the CL1_ACK Counter reaches a count of tEnterCLx, the Re-timer Lane Adapter shall: Transition the Re-timer Channel transmitter to electrical idle within tTxOff time from expiration of the CL1_ACK Counter.
4.2.4.1#14rt	NT	When the CL1_ACK Counter reaches a count of tEnterCLx, the Re-timer Lane Adapter shall: Wait tEnterLFPS1, then enable detection of Low Frequency Periodic Signaling (LFPS).
4.2.4.1#15rt	NT	On detection of 3 back-to-back CL_OFF Ordered Sets, the Re-timer Lane Adapter shall start counting time in Symbol Time units.
4.2.4.1#16rt	NT	The initial value of CL_OFF Counter shall be the number of CL_OFF Ordered Set Symbols that were already forwarded.
4.2.4.1#17rt	NT	While the receiver is shut down and the Channel still in Forwarding state, the transmitter shall transmit a DC balanced signal and may use local clock without SSC.
4.2.4.1#18rt	NT	When the CL_OFF Counter reaches a count of tEnterCLx, the Re-timer Lane Adapter shall: Transition the Re-timer Channel in the direction forwarding the CL_OFF Ordered Sets to a low power state as follows: If CL2_ACK Ordered Sets were detected during the entry flow, transition to CL2 state; If CL1_ACK Ordered Sets were detected during the entry flow, transition to CL1 state; If CL0s_ACK Ordered Sets were detected during the entry flow, transition to CL0s state.
4.2.4.1#19rt	NT	When the CL_OFF Counter reaches a count of tEnterCLx, the Re-timer Lane Adapter shall: Reset the CL_OFF Counter.
4.2.4.1#20rt	NT	When the CL_OFF Counter reaches a count of tEnterCLx, the Re-timer Lane Adapter shall: Transition the Re-timer Channel transmitter to electrical idle within tTxOff time from expiration of the CL_OFF Counter.
4.2.4.1#21rt	NT	When the CL_OFF Counter reaches a count of tEnterCLx, the Re-timer Lane Adapter shall: Wait tEnterLFPS1, then enable detection of Low Frequency Periodic Signaling (LFPS).
4.2.4.1#22rt	NT	A Re-timer Lane Adapter shall respond to Logical Layer Errors as defined in Section 4.3.1.
4.2.4.1#23rt	NT	If a Re-timer Lane Adapter detects 15 back-to-back SLOS Symbols, it shall abort the entry flow.

4.2.4.1#24rt	NT	The Re-timer Lane Adapter shall also reset the CL2_ACK Counter and the CL1_ACK Counter to zero.
<b>4.2.4.2 Behavior in State</b>		
4.2.4.2#1rt	TD 4.011	While a Re-timer Channel is in CL2 state, its transmitter shall be in electrical idle. Lane common mode voltages shall be maintained.
4.2.4.2#2rt	TD 4.013	While a Re-timer Channel is in CL1 state, its transmitter shall be in electrical idle. Lane common mode voltages shall be maintained.
4.2.4.2#3rt	TD 4.015	While a Re-timer Channel is in CL0s state, its transmitter shall be in electrical idle. Lane common mode voltages shall be maintained.
<b>4.2.4.3 Exit from State</b>		
<b>4.2.4.3.1 CL0s Exit</b>		
4.2.4.3.1#1rt	NT	When a Re-timer detects an LFPS burst on one of its receivers, the Re-timer shall: Send a Low Frequency Periodic Signaling (LFPS) burst from the Corresponding Transmitter. The duration of the LFPS burst shall be at least 16 LFPS cycles and no more than tLFPSDuration.
4.2.4.3.1#2rt	NT	When a Re-timer detects an LFPS burst on one of its receivers, the Re-timer shall: Return the Corresponding Transmitter to Electrical Idle for tPreData.
4.2.4.3.1#3rt	TD 4.015	When a Re-timer detects an LFPS burst on one of its receivers, the Re-timer shall: Enable the receiver to start calibration. The Re-timer shall not enable the receiver until at least tIdleRx after the last LFPS cycle was received.
4.2.4.3.1#4rt	NT	When a Re-timer detects an LFPS burst on one of its receivers, the Re-timer shall: Start sending CL_WAKE1.X Ordered Set Symbols from the Corresponding Transmitter, where X is the Re-timer Index assigned by the Router that is the target of the CL_WAKE1.X Ordered Set Symbols. The Re-timer shall transmit the Symbols using a locally generated, non-SSC, clock.
4.2.4.3.1#5rt	NT	After a Re-timer receives 3 back-to-back CL_WAKE2.X Ordered Set Symbols (where X is the same value as in step 4) on at least one Lane Adapter, the Re-timer shall transition each Re-timer Channel that is in CL0s state to transmit on the clock recovered from the received Symbols rather than on its local clock.
4.2.4.3.1#6rt	NT	The transition shall happen only after bit lock is achieved by all Re-timer Channels that are in CL0s state.
4.2.4.3.1#7rt	TD 4.015	Each Re-timer Channel in CL0s state shall transition to Forwarding state. From this point on, a Re-timer Channel shall forward the bit stream it receives from the Lane and stop generating CL_WAKE1.X Ordered Set Symbols.
4.2.4.3.1#8rt	NT	During the transition from local clock to receiver clock, the Re-timer shall meet the SSC_SLEW_RATE requirement as specified in the USB4 Base Specification.



<b>4.2.4.3.2 CL1/CL2 Exit</b>		
<b>4.2.4.3.2.1 Phase 1</b>		
4.2.4.3.2.1#1rt	TD 4.011 TD 4.013	When a Re-timer detects an LFPS burst of 2 cycles on one of its Lane Adapters, it shall do the following: 1. Send LFPS as follows: The Lane Adapter that detected the LFPS shall send LFPS for at least 5 LFPS cycles and no more than tLFPSDuration.
4.2.4.3.2.1#2rt	NT	When a Re-timer detects an LFPS burst of 2 cycles on one of its Lane Adapters, it shall do the following: 1. Send LFPS as follows: The Corresponding Adapter shall send LFPS until it detects LFPS.
4.2.4.3.2.1#3rt	NT	When a Re-timer detects an LFPS burst of 2 cycles on one of its Lane Adapters, it shall do the following: 2. Enable the receivers for the Lane Adapter and its Corresponding Adapter.
4.2.4.3.2.1#4rt	TD 4.011 TD 4.013	The Re-timer shall wait at least tIdleRx after a Lane Adapter stops detecting LFPS before enabling the receiver for that Lane Adapter.
4.2.4.3.2.1#5rt	TD 4.011 TD 4.013	For each Adapter, after the last LFPS is transmitted, transition the transmitter to Electrical Idle for tPreData. Then, start transmitting CL_WAKE1.X Ordered Set Symbols, where X is the index of the Re-timer provided by the Router that is the target of the CL_WAKE1.X Ordered Set Symbols.
4.2.4.3.2.1#6rt	NT	The Re-timer shall transmit the Symbols using a locally generated, non-SSC, clock.
<b>4.2.4.3.2.2 Phase 2</b>		
4.2.4.3.2.2#1rt	NT	When a Re-timer receives 3 CL_WAKE2.(X+1) Symbols (where X is the Re-timer Index programmed by the Router that is the source of the CL_WAKE2.(X+1) Symbols), and if the Re-timer is still transmitting on its local clock in this Re-timer Channel, then the Re-timer shall transition this Re-timer Channel to toggle between transmitting two locally-generated CL_WAKE1.X Ordered Set Symbols and transmitting the last two CL_WAKE2.Y Symbols received by the Re-timer Channel.
4.2.4.3.2.2#2rt	NT	CL_WAKE1 Symbols received by the Port shall not be transmitted while the Port is in toggling mode.
<b>4.2.4.3.2.3 Phase 3</b>		
4.2.4.3.2.3#1rt	NT	After a Re-timer receives 3 back-to-back CL_WAKE2.X Symbols (where X is the Re-timer Index programmed by the Router that is the source of the CL_WAKE2.X Symbols) on Lane 0 of a Re-timer Channel in a given direction, the Re-timer shall transition all Re-timer Channels in the opposite direction to transmit on the clock recovered from the received traffic rather than on its local clock.

4.2.4.3.2.3#2rt	NT	A Re-timer Channel shall ignore any received CL_WAKE1.Y (where Y is any value) Symbols interleaved with CL_WAKE2.X Ordered Set Symbols when it determines the reception of back-to-back CL_WAKE2.X Ordered Set Symbols.
4.2.4.3.2.3#3rt	NT	The transition shall happen only after bit lock is achieved by both active receivers in the Re-timer Channel performing the transition.
4.2.4.3.2.3#4rt	TD 4.011 TD 4.013	Each Re-timer Channel performing the transition shall transition to Forwarding state. From this point on, the Re-timer Channel shall forward the bit stream it receives from the Lane and stop generating CL_WAKE1.X Ordered Set Symbols.
4.2.4.3.2.3#5rt	NT	During the transition from local clock to receiver clock, the Re-timer Channel shall meet the SSC_SLEW_RATE requirement as specified in the USB4 Base Specification.
<b>4.2.4.3.3 Timing Requirements</b>		
4.2.4.3.3#1rt	NT	A Re-timer shall meet the following timing requirements during exit from CL0, CL1, or CL2 states:
4.2.4.3.3#2rt	TD 4.011 TD 4.013 TD 4.015	A receiver shall complete Symbol lock within tCLxLock of receiving SLOS or CL_WAKE1.X Ordered Set Symbols.
4.2.4.3.3#3rt	NT	A transmitter shall complete the transition to a recovered clock within tSwitchNoSSC if the received clock is a non-SSC clock.
4.2.4.3.3#4rt	NT	A transmitter shall complete the transition to a recovered clock within tSwitchSSC if the received clock is an SSC clock.
<b>4.3 Lane Decoding</b>		
4.3#1rt	NT	To track entry into CLx states and to participate in exit from CLx states, a Re-timer shall decode Ordered Sets received on its Lane Adapters as defined in the USB4 Specification.
<b>4.3.1 Error Cases</b>		
4.3.1#1rt	NT	Table 4-4 lists the error cases that a Re-timer shall support along with how that error shall be handled.
4.3.1#2rt	NT	If Lane Adapter detects 3 SLOS in Forwarding state with RS-FEC on or Lane Adapter detects 15 SLOS in Forwarding state with RS-FEC off, it is a SLOS Detection Error. If RS-FEC decoding is on, turn-off RS-FEC decoding on this Lane in both USB4 Ports and perform Symbol lock on received SLOS
4.3.1#3rt	NT	If The RS-FEC decoder identifies an uncorrectable error, it is an RS-FEC Decoder error. Turn off RS-FEC decoding on this Lane. Perform Symbol lock on received SLOS.

#### **4.4 Timing Parameters**

## Chapter 6

The following Table presents the USB4 Re-timer Specification Chapter 6 asserts.

Assertion #	Test Name	Assertion Description
<b>6 Interoperability with Thunderbolt™ 3 (TBT3) Systems</b>		
6#1rt	NT	A Cable Re-timer shall support the requirements defined in this chapter.
<b>6.2 Logical Layer</b>		
<b>6.2.1 Sideband Channel</b>		
6.2.1#1rt	NT	This section defines the additional Sideband Channel behavior that a Re-timer shall implement when operating in a TBT3-Compatible that uses a TBT3-Compatible Sideband Channel
<b>6.2.1.1 Bidirectional Re-timers</b>		
<b>6.2.1.1.1 Cable Re-timers</b>		
6.2.1.1.1#1rt	IOP	A Cable Re-timer shall implement a unidirectional behavior when the Sideband Channel operates in TBT3-Compatible mode.
<b>6.2.1.1.2 On-Board Re-timers</b>		
6.2.1.1.2#1rt	NT	An On-Board Re-timer that is adjacent to a USB Type-C connector shall implement both unidirectional and bidirectional behavior.
6.2.1.1.2#2rt	IOP	When the Re-timer is adjacent to a Thunderbolt Cable Re-timer, it shall operate as a bidirectional Re-timer on its Cable-Facing USB4 Port. The Router-Facing USB4 Port shall operate as a unidirectional Re-timer.
6.2.1.1.2#3rt	IOP	When the Re-timer is not adjacent to a Thunderbolt Cable Re-timer, it shall operate as a unidirectional Re-timer on both USB4 Ports.
6.2.1.1.2#4rt	IOP	An On-Board Re-timer that is not adjacent to a USB Type-C connector shall implement unidirectional behavior on both USB4 Ports.
6.2.1.1.2#5rt	NT	When a USB4 Port on an On-Board Re-timer is operating in bidirectional mode: The USB4 Port shall support concurrent reception of Transactions on SBTX and on SBRX.
6.2.1.1.2#6rt	NT	When a USB4 Port on an On-Board Re-timer is operating in bidirectional mode: The USB4 Port shall drive its SBTX for up to 2 bit times after the last Stop bit of an AT Command.
6.2.1.1.2#7rt	NT	When a USB4 Port on an On-Board Re-timer is operating in bidirectional mode: The USB4 Port shall not forward a received Transaction if it is still waiting for a Response to a RT Command it sent.

<b>6.2.1.2 Transactions</b>		
<b>6.2.1.2.1 LT Transactions</b>		
6.2.1.2.1#1rt	IOP	A Re-timer shall forward an LT_Resume Transaction received on one USB4 Port to its other USB4 Port.
6.2.1.2.1#2rt	IOP	A Cable Re-timer shall forward an LT_Resume2 Transaction received on its Router-Facing USB4 Port to its Cable-Facing USB4 Port.
6.2.1.2.1#3rt	IOP	A Re-timer shall forward a received LT_Gen_2 Transaction to its other USB4 Port.
6.2.1.2.1#4rt	IOP	A Re-timer shall forward a received LT_Gen_3 Transaction to its other USB4 Port.
<b>6.2.1.2.2 AT Transactions</b>		
<b>6.2.1.2.2.1 Cable Re-timers</b>		
6.2.1.2.2.1#1rt	NT	A Cable Re-timer shall support the Bounce mechanism as defined in the USB4 Specification.
6.2.1.2.2.1#2rt	NT	A Cable Re-timer shall not initiate AT Commands.
6.2.1.2.2.1#3rt	NT	A Cable Re-timer shall respond to a received AT Command that has the Recipient bit set to 0b and the <i>Bounce</i> bit set to 0b.
6.2.1.2.2.1#4rt	NT	Else, it shall forward the received AT Command to its other USB4 Port.
<b>6.2.1.2.2.2 On-Board Re-timers</b>		
6.2.1.2.2.2#1rt		An On-Board Re-timer shall respond to a received AT Command with the <i>Recipient</i> bit set to 1b that access the TxFFE Register in the SB Register Space.
6.2.1.2.2.2#2rt		It shall forward other received AT Commands to its other USB4 Port.
6.2.1.2.2.2#3rt		An On-Board Re-timer shall process to a received AT Response with the <i>Recipient</i> bit set to 1b that access the TxFFE Register in the SB Register Space.
6.2.1.2.2.2#4rt		It shall not forward the AT Response to its other USB4 Port.
6.2.1.2.2.2#5rt		It shall forward other received AT Responses to its other USB4 Port.
<b>6.2.1.2.3 RT Transactions</b>		
6.2.1.2.3#1rt	NT	An On-Board Re-timer that is adjacent to a USB Type-C connector shall not forward Broadcast RT Transactions towards the cable.

6.2.1.2.4 SB Register Space		
6.2.1.2.4#1rt	TBD	The SB Register Space of a Re-timer shall have the additional fields described in Table 6-1 and Table 6-2.
6.2.1.3 Lane Initialization		
6.2.1.3.1 Phase 1 – Determination of Initial Conditions		
6.2.1.3.2 Phase 2 – Lane Parameters Synchronization		
6.2.1.3.2#1rt	IOP	An On-Board Re-timer shall decode Broadcast RT Transactions, LT_Gen_2 Transactions, and LT_Gen_3 Transactions, and shall use the Link parameter from the most recently received Transaction.
6.2.1.3.2#2rt	NT	A Cable Re-timer shall decode LT_Gen_2 Transactions and LT_Gen_3 Transactions, and shall use the Link parameter from the most recently received LT Transaction.
6.2.1.3.2#3rt	NT	If, on any USB4 Port, a Cable Re-timer detects LT_Resume for Lane 0 before it detects at least one LT_Gen_2 Transaction or LT_Gen_3 Transaction for Lane 1, then the Re-timer shall keep the Lane 1 Adapters in both USB4 Ports in the CLd state and shall not proceed with Lane Initialization.
6.2.1.3.2#4rt	IOP	When a Re-timer detects LT_Resume on any Lane of any USB4 Port, it shall transition to phase 5.
6.2.1.3.3 Phase 3 – Lane Equalization		
6.2.1.3.3#1rt	IOP	Table 6-3 lists which TxFFE negotiation flows a transmitter or receiver shall perform in phase 5.
6.2.1.3.3#2rt	NT	An On-Board Re-timer Lane Adapter that is not adjacent to a USB Type-C connector shall turn on its transmitter when the <i>Rx Active</i> bit of its Corresponding Receiver is set to 1b.
6.2.1.3.3#3rt	NT	An On-Board Re-timer Lane Adapter that is not adjacent to a USB Type-C connector: It shall start transmitting CL_WAKE1.X Ordered Set Symbols, where X is the Re-timer Index assigned by the Router that is the target of the CL_WAKE1.X Ordered Set Symbols.
6.2.1.3.3#4rt	NT	An On-Board Re-timer Lane Adapter that is not adjacent to a USB Type-C connector: The transmitter shall use a locally generated, non-SSC clock to transmit the CL_WAKE1.X Ordered Set Symbols.
6.2.1.3.3#5rt	NT	An On-Board Re-timer Lane Adapter that is not adjacent to a USB Type-C connector: It shall then set the <i>Tx Active</i> bit for the Lane Adapter to 1b.
6.2.1.3.3#6rt	NT	A Re-timer adjacent to a USB Type-C connector shall set the <i>Clock Switch Done</i> bit to 1b in a Router-Facing Adapter when all receivers in Router-Facing Adapters complete TxFFE negotiation.

6.2.1.3.3#7rt	NT	Once the <i>Clock Switch Done</i> bit is set to 1b, a transmitter adjacent to a USB Type-C connector that is turned on shall forward the bit stream it receives from the Corresponding Receiver using a recovered clock.
6.2.1.3.3#8rt	NT	When all of the following are true, a transmitter that is not adjacent to a USB Type-C connector shall stop using the local clock, shall start using the recovered clock from the Corresponding Receiver, and shall forward the bit stream it receives from the Corresponding Receiver: In the transmitter's USB4 Port, TxFFE negotiation is complete between all transmitters and their Adjacent Receivers; In the USB4 Port opposite the transmitter's USB4 Port, TxFFE negotiation is complete between all receivers and their Adjacent Transmitter; The <i>Clock Switch Done</i> bit for Lane 0 of the transmitter's adjacent USB4 Port is 1b.
6.2.1.3.3#9rt	NT	A Re-timer adjacent to a Router shall set the <i>Forward Switch Done</i> bit to 1b in a Lane Adapter of a Cable-Facing USB4 Port when transmitter of the Lane Adapter is using the receiver clock from the Corresponding Receiver.
6.2.1.3.3#10rt	NT	A Re-timer shall set the <i>Forward Switch Done</i> bit to 1b in a Lane Adapter if the <i>Forward Switch Done</i> bit is set to 1b in the adjacent USB4 Port of the Corresponding Receiver.
6.2.1.3.3#11rt	NT	When the <i>Forward Switch Done</i> bit is set to 1b in an adapter adjacent to a USB Type-C connector, the Lane Adapter shall turn on its transmitter, if it has not done so already. It shall then set the <i>Tx Active</i> bit to 1b and perform TxFFE Parameter Negotiation.
6.2.1.3.3#12rt	NT	When an On-Board Re-timer transmitter completes TxFFE negotiation with a Cable Re-timer receiver, the transmitter shall send an LT_Resume2 Transaction. The <i>LSELane</i> field in the LT_Resume2 Transaction shall equal the Lane number associated with the transmitter.
6.2.1.3.3#13rt	NT	A Cable Re-timer shall set the <i>Tx Active</i> bit to 1b in a Router-Facing Adapter when the Lane Adapter is transmitting the bit stream received by a Lane Adapter at the other end of the Cable, and transmission uses the recovered clock from the Lane Adapter at the other end of the Cable.
<b>6.2.1.3.3.1 Asymmetric TxFFE Parameter Negotiation with a Receiving Subordinate Partner</b>		
<b>Receiver flow:</b>		
6.2.1.3.3.1#1rt	IOP	The steps that the receiver shall perform to complete negotiation are listed below:
6.2.1.3.3.1#2rt	NT	1) The receiver shall set the following initial values on entry to Phase 5: Local <i>Rx Status &amp; TxFFE Request</i> byte of the <i>TxFFE</i> register: <i>Rx Locked</i> bit = 0b; <i>TxFFE Request</i> field = index of an initial set of TxFFE parameters; <i>Rx Active</i> bit = 0b; <i>New Request</i> bit = 0b; <i>Partner Tx Status</i> byte of the <i>TxFFE</i> register: <i>Tx Active</i> bit = 0b; <i>Request Done</i> bit = 0b.

6.2.1.3.3.1#3rt	NT	2) The receiver shall evaluate the value of the <i>Tx Active</i> bit in the <i>Partner Tx Status</i> byte of the <i>TxFFE</i> register: If <i>Tx Active</i> = 1b (i.e. the transmitter is transmitting), then the receiver shall enable the receiver, set <i>Rx Active</i> bit to 1b, and continue to Step 3.
6.2.1.3.3.1#4rt	NT	2) The receiver shall evaluate the value of the <i>Tx Active</i> bit in the <i>Partner Tx Status</i> byte of the <i>TxFFE</i> register: Else, repeat Step 2 within tPollTxFFE.
6.2.1.3.3.1#5rt	NT	3) The receiver shall evaluate its behavior. If equalization is complete, the receiver shall set the <i>Rx Locked</i> field in the <i>Local Rx Status &amp; TxFFE Request</i> byte to 1b
6.2.1.3.3.1#6rt	NT	4) The receiver shall do the following: If the <i>Rx Locked</i> bit is set to 1b, negotiation is complete and no further TxFFE negotiation steps shall be taken.
6.2.1.3.3.1#7rt	NT	4) The receiver shall do the following: Else: <i>TxFFE Request</i> field shall be set to the index of a selected set of TxFFE parameters; <i>New Request</i> bit shall be set to 1b to indicate the receiver is providing a new TxFFE index.
6.2.1.3.3.1#8rt	NT	5) Continue to Step 6 only after sending a read Response with the updated values of its TxFFE Register.
6.2.1.3.3.1#9rt	NT	6) On reception of an AT Command with a write Command targeting its <i>Partner Tx Status</i> byte of the <i>TxFFE</i> register, the receiver shall: If ( <i>Tx Active</i> = 1b) AND ( <i>TxFFE setting</i> = value of <i>TxFFE Request</i> in the <i>Local Rx Status &amp; TxFFE Request</i> byte), go to Step 7.
6.2.1.3.3.1#10rt	NT	6) On reception of an AT Command with a write Command targeting its <i>Partner Tx Status</i> byte of the <i>TxFFE</i> register, the receiver shall: Else, repeat Step 6.
6.2.1.3.3.1#11rt	NT	7) The receiver shall evaluate its receiver behavior. If equalization is complete, the receiver shall set the <i>Rx Locked</i> field in the <i>Local Rx Status &amp; TxFFE Request</i> byte to 1b.
6.2.1.3.3.1#12rt	NT	8) The receiver shall set the <i>New Request</i> field in the <i>Local Rx Status &amp; TxFFE Request</i> byte to 0b.
6.2.1.3.3.1#13rt	NT	9) On reception of an AT command with a read Command targeting the TxFFE register go to Step 4.
<b>6.2.1.3.3.2 – Asymmetric TxFFE Parameter Negotiation with a Transmitting Subordinate Partner</b>		
<b>Transmitter flow:</b>		
6.2.1.3.3.2#1rt	IOP	The steps that the transmitter shall perform to complete negotiation are listed below:
6.2.1.3.3.2#2rt	NT	1) The transmitter shall set the following initial values on entry to Phase 5: <i>Local Tx Status</i> byte of the TxFFE register: <i>Tx Active</i> bit = 1b; <i>Request Done</i> bit = 0b; <i>TxFFE Setting</i> field = index of an initial set of TxFFE parameters; <i>Partner Rx Status &amp; TxFFE Request</i> byte of the TxFFE register: <i>New Request</i> bit = 0b.



6.2.1.3.3.2#3rt	NT	2) On reception of an AT Command with a write Command targeting the <i>Partner Rx Status &amp; TxFFE Request</i> byte of the <i>TxFFE</i> register, the transmitter shall: If ( <i>New Request</i> = 0b), repeat Step 2.
6.2.1.3.3.2#4rt	NT	2) On reception of an AT Command with a write Command targeting the <i>Partner Rx Status &amp; TxFFE Request</i> byte of the <i>TxFFE</i> register, the transmitter shall: Else, continue to Step 3.
6.2.1.3.3.2#5rt	NT	3) Load one of 16 predefined <i>TxFFE</i> configurations that matches the <i>TxFFE Request</i> field of the received AT Command.
6.2.1.3.3.2#6rt	NT	4) Send an AT Response to indicate the transmitter is using the new <i>TxFFE</i> request.
6.2.1.3.3.2#7rt	NT	5) On reception of an AT Command with a write Command targeting the <i>Partner Rx Status &amp; TxFFE Request</i> byte of the <i>TxFFE</i> register, the transmitter shall: If ( <i>New Request</i> = 1b), repeat Step 4.
6.2.1.3.3.2#8rt	NT	5) On reception of an AT Command with a write Command targeting the <i>Partner Rx Status &amp; TxFFE Request</i> byte of the <i>TxFFE</i> register, the transmitter shall: Else, continue to Step 2.
<b>6.2.2 Re-timer Channel State Machine</b>		
<b>6.2.2.1 CLd State</b>		
<b>6.2.2.1.1 Behavior in State</b>		
6.2.2.1.1#1rt	NT	In addition to the conditions described in Section 4.2.1.2, a Re-timer Channel shall begin Lane Initialization in phase 4 when: If the Re-timer Channel entered this state after detecting an <i>LT_Fall</i> Transaction, then: The Re-timer Channel for Lane 0 shall start Lane Initialization when the Re-timer receives a Broadcast RT Transaction with the <i>Lane0 Enabled</i> bit set to 1b, an <i>LT_Gen_2</i> Transaction with the <i>LSELane</i> bit set to 0b, or an <i>LT_Gen_3</i> Transaction with the <i>LSELane</i> bit set to 0b.
6.2.2.1.1#2rt	NT	In addition to the conditions described in Section 4.2.1.2, a Re-timer Channel shall begin Lane Initialization in phase 4 when: If the Re-timer Channel entered this state after detecting an <i>LT_Fall</i> Transaction, then: The Re-timer Channel for Lane 1 shall start Lane Initialization when the Re-timer receives a Broadcast RT Transaction with the <i>Lane1 Enabled</i> bit set to 1b, an <i>LT_Gen_2</i> Transaction with the <i>LSELane</i> bit set to 1b, or an <i>LT_Gen_3</i> Transaction with the <i>LSELane</i> bit set to 1b.

## Test Requirements

### Hardware

Vendor provides the Unit Under Test (UUT) in a reference system for testing. The reference system must expose one USB Type-C™ connector per USB4™ Port. The USB Type-C connector is the test point for the UUT.

For a USB4 host:

- Reference system must be x64-based or ARM64-based, run Windows 10 or later
- Host Router must be PCIe-based or ACPI-based
- The Reference System must include a way to connect to the Analyzer/Exerciser. This is to allow the Analyzer/Exercise hardware and software to operate concurrently on the same system with USB4 CV while USB4 CV controls the USB4 hardware.

*Note: In the future, will expand host testing to other OS and architectures.*

### Timing

Exerciser adds additional time to simulate 2 Cable Re-timers and 2 On-Board Re-timers (worst case latency) on the Link between Exerciser and UUT. The total roundtrip latency is calculated as follows:

$$\text{Total Latency} = 2 (\# \text{ of Re-timers}) (\text{individual Re-timer Latency})$$

For Gen 2 speeds, the Exerciser adds 400 ns delay:

$$\text{Total Latency} = 2(4)(50 \text{ ns}) = 400 \text{ ns}$$

For Gen 3 speeds, the Exerciser adds 240 ns delay:

$$\text{Total Latency} = 2(4)(30 \text{ ns}) = 240 \text{ ns}$$

### Product

The Vendor Info File (VIF) is used in conjunction with test software to indicate RUT product implementation. This file can be generated using the following tool:

<http://www.usb.org/developers/tools/#PDFFile>

<https://www.usb.org/document-library/usb-vendor-info-file-generator-version-2010>

*Note: The VIF may be generated by test equipment vendors as well.*

## USB4 Mode Test Setups

This section defines the test setups for a Router Assembly that is part of a USB4™ host, hub, or device. The test setups in this section are used for the USB4 Mode Tests.

A USB4-Based Dock is tested as a USB4 hub.

### Notes and Best Practices

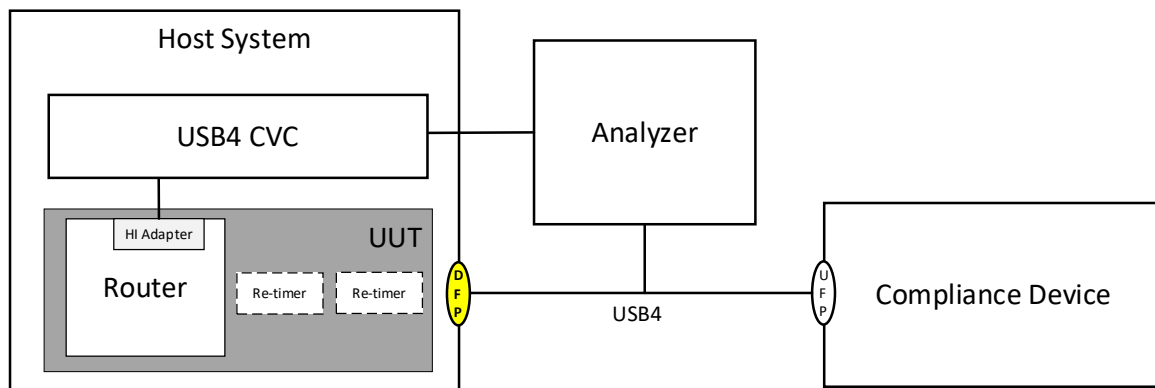
- When using the Teledyne LeCroy Voyager M4x as the USB4 Analyzer or USB4 Exerciser, use the “short” USB4 cables included with the M4x. The eMarked cable should be used to connect the USB4 DFP (Host or Hub) to the M4x and the non-eMarked cable should be used to connect a USB4 Hub, Dock, or Device to the M4x.

### Host

This section describes the test setups for a Router Assembly that is part of a USB4 host. The Port Under Test (PUT) is highlighted in each figure.

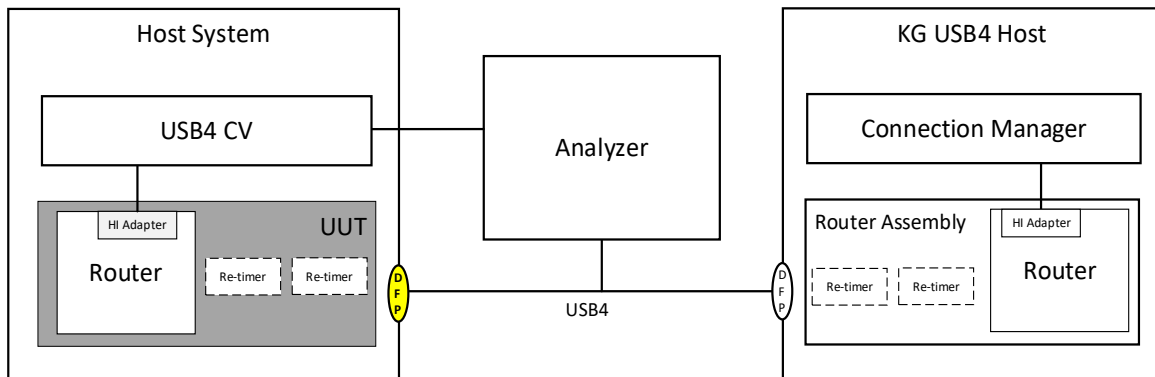
#### AN\_HOST\_DFP1

- A Compliance Device is connected to the DFP of the UUT
- USB4 CV is installed on the Host System with the UUT
- A USB4 Analyzer is connected between the UUT and Compliance Device



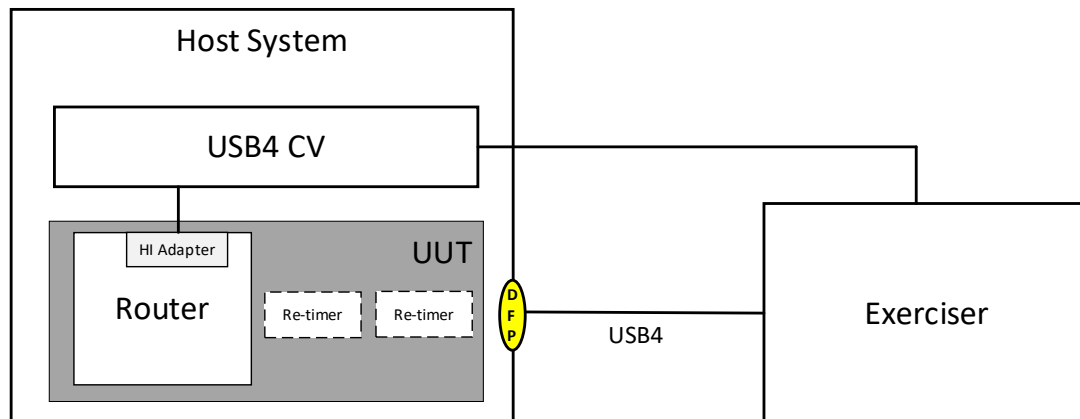
## AN\_HOST\_DFP2

- A KG USB4 host is connected to the UUT
- USB4 CV is installed on the Host System with the UUT
- A USB4 Analyzer is connected between the UUT and KG USB4 Host



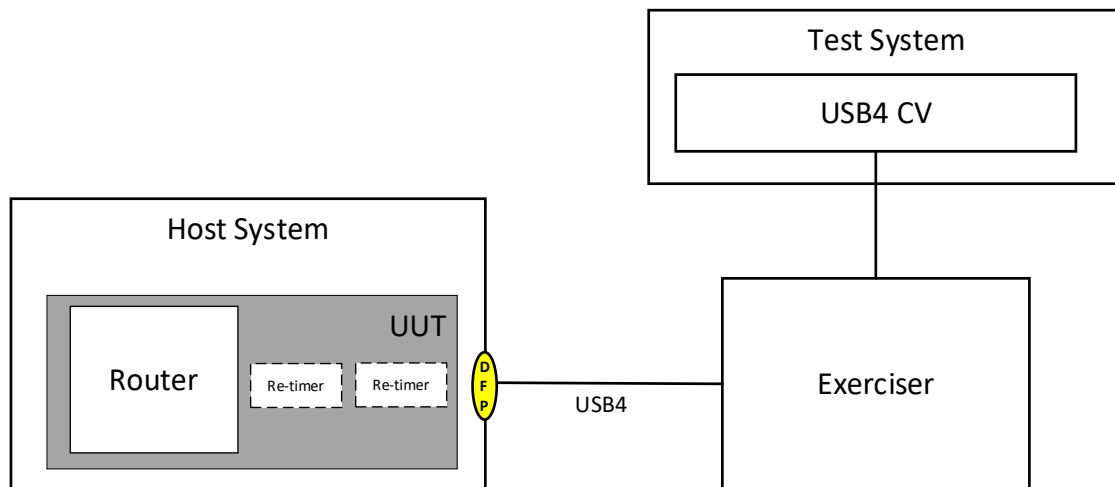
## EX\_HOST\_DFP1

- The Exerciser is connected to the UUT
- Unless specified otherwise, the Exerciser is in USB4 device mode and presents as UFP
- USB4 CV is installed on the Host System with the UUT



## EX\_HOST\_DFP2

- The Exerciser is connected to the UUT
- Unless specified otherwise, the Exerciser is in USB4 device mode and presents as UFP
- USB4 CV is installed on a separate system (Test System) than the UUT
- The Test System connects to the Exerciser via a separate connection



## DC\_HOST\_DFP1

- A Compliance Device is connected to the DFP of the UUT
- USB4 CV is installed on the Host System with the UUT
- Test steps that require an Analyzer are skipped

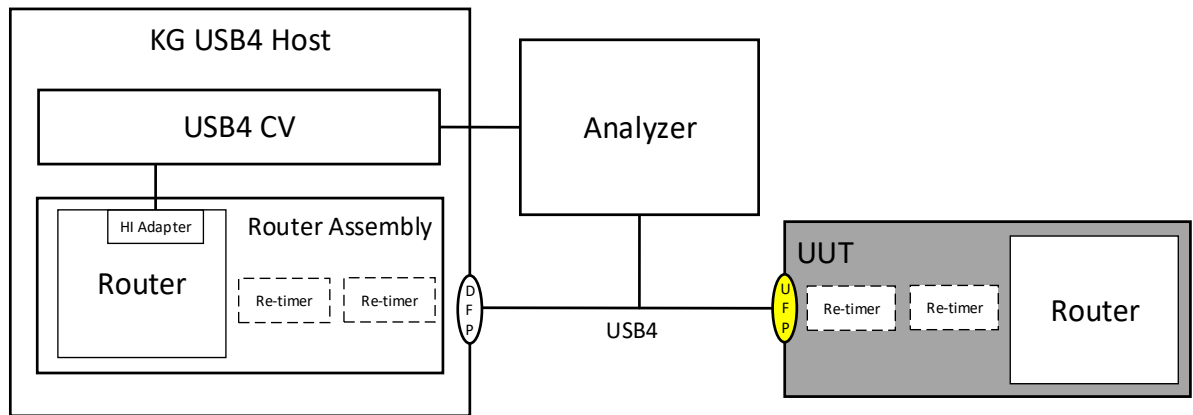
[OBJ]

## Hub

This section describes the test setups for a Router Assembly that is part of a USB4 hub. The Port Under Test (PUT) is highlighted in each figure.

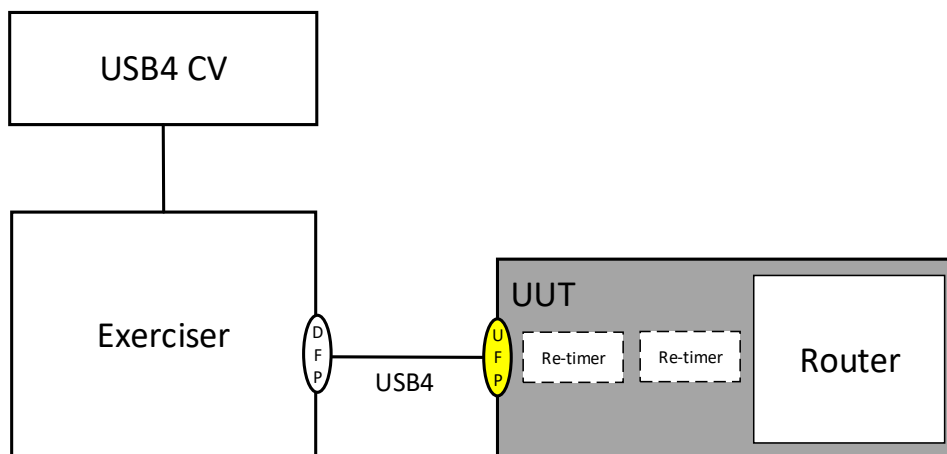
### AN\_HUB\_UFP1

- A KG USB4 Host is connected to the UUT
- USB4 CV is installed on the KG Host System
- A USB4 Analyzer is connected between the UUT and Compliance Device



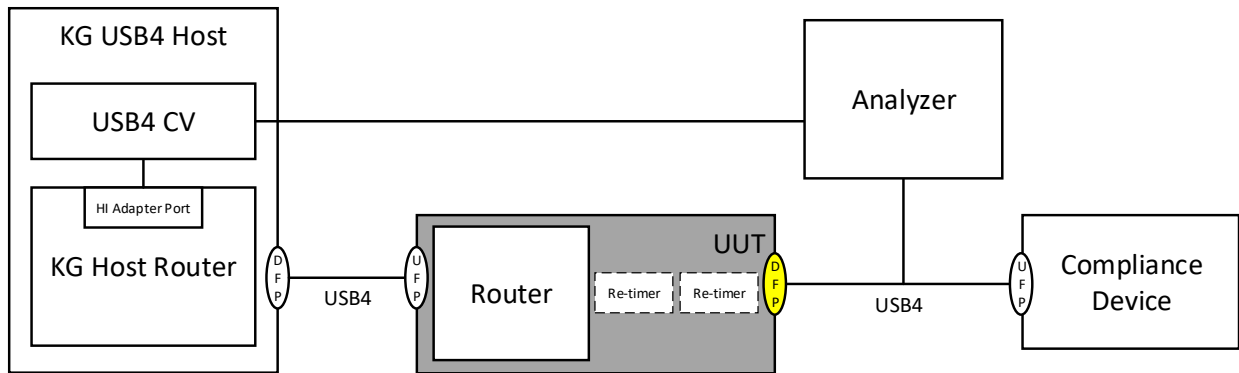
### EX\_HUB\_UFP1

- The Exerciser is connected to the UUT
- Exerciser is configured as a USB4 DFP



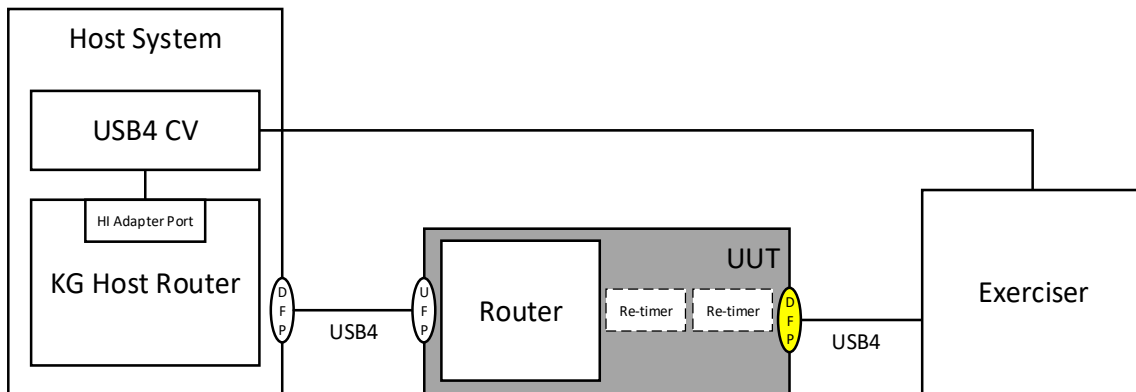
## AN\_HUB\_DFP1

- A KG USB4 host is connected to the UFP of the UUT
- A Compliance Device is connected to the DFP of the UUT
- USB4 CV is installed on the KG Host System
- A USB4 Analyzer is connected between the UUT and Compliance Device



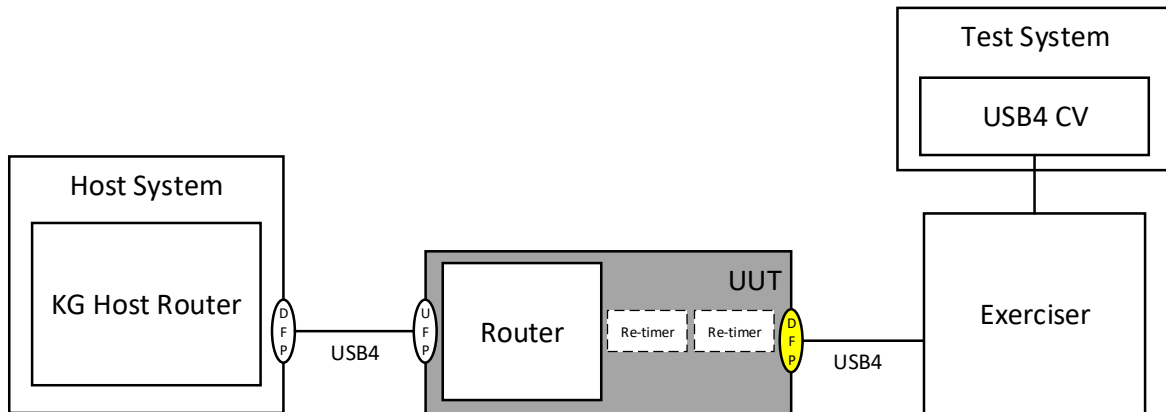
## EX\_HUB\_DFP1

- A KG USB4 host is connected to the UFP of the UUT
- The Exerciser is connected to the DFP of the UUT
- Unless otherwise specified, the Exerciser is in USB4 Device mode and presents as a UFP



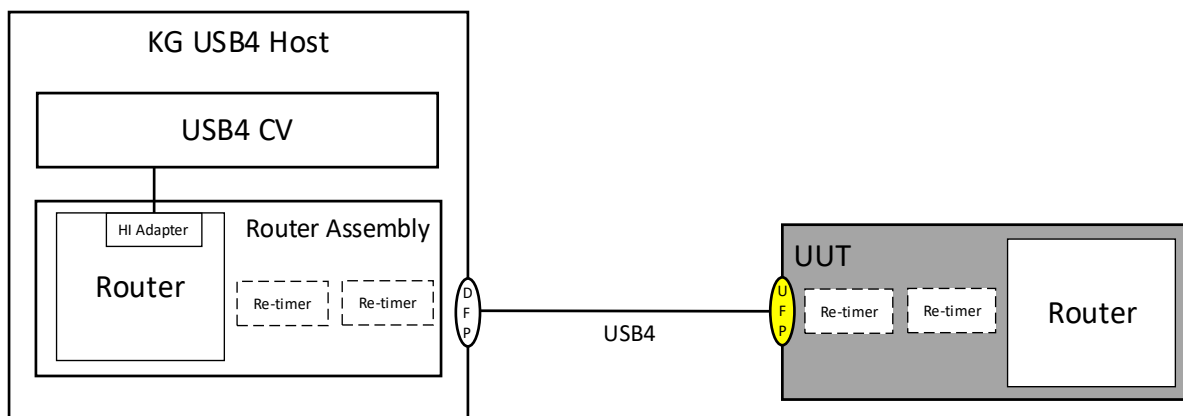
## EX\_HUB\_DFP2

- A KG USB4 host is connected to the UFP of the UUT
- The Exerciser is connected to the DFP of the UUT
- Unless otherwise specified, the Exerciser is in USB4 Device mode and presents as a UFP
- The Test System connects to the Exerciser via a separate connection



## DC\_HUB\_UFP1

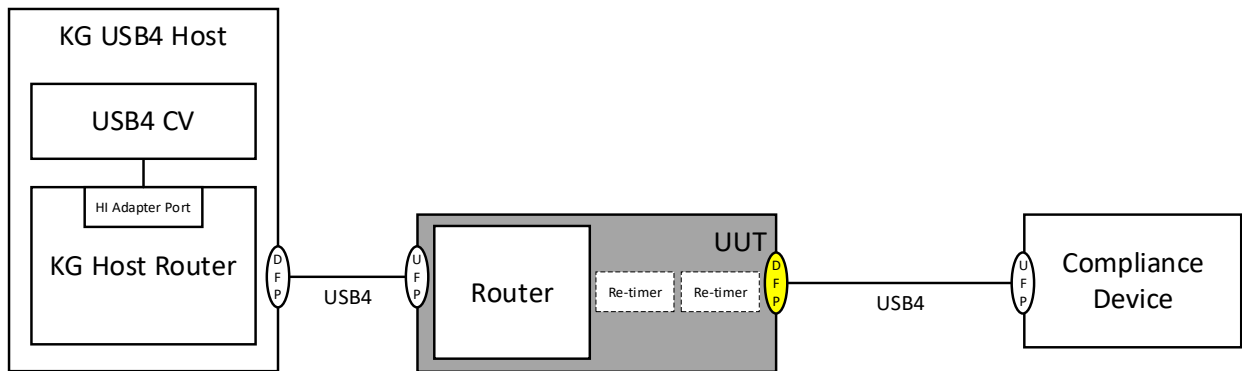
- A KG USB4 Host is connected to the UUT
- USB4 CV is installed on the KG Host System
- Test steps that require an Analyzer are skipped





## DC\_HUB\_DFP1

- A KG USB4 host is connected to the UFP of the UUT
- A Compliance Device is connected to the DFP of the UUT
- USB4 CV is installed on the KG Host System
- Test steps that require an Analyzer are skipped

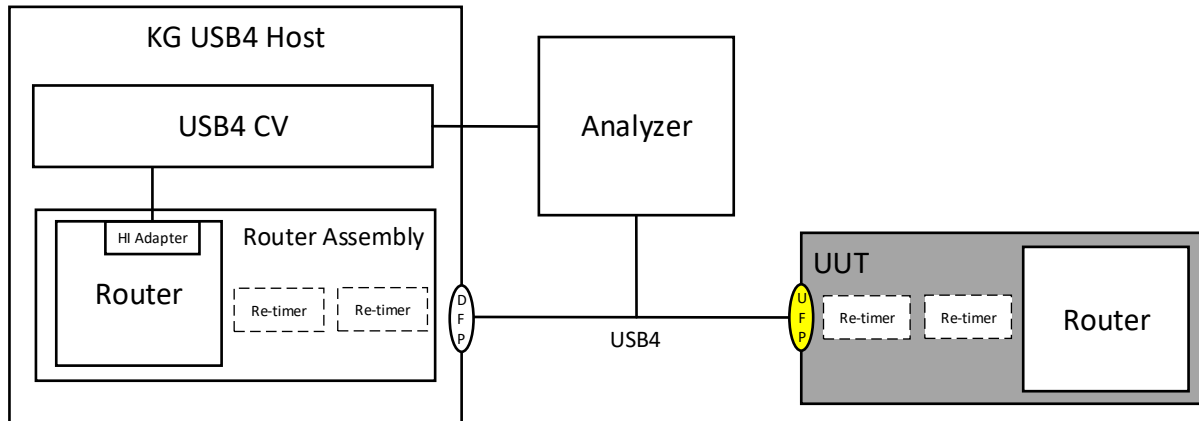


## Peripheral Device

This section describes the test setup for a Router Assembly that is part of a USB4 device. The Port Under Test (PUT) is highlighted in each figure.

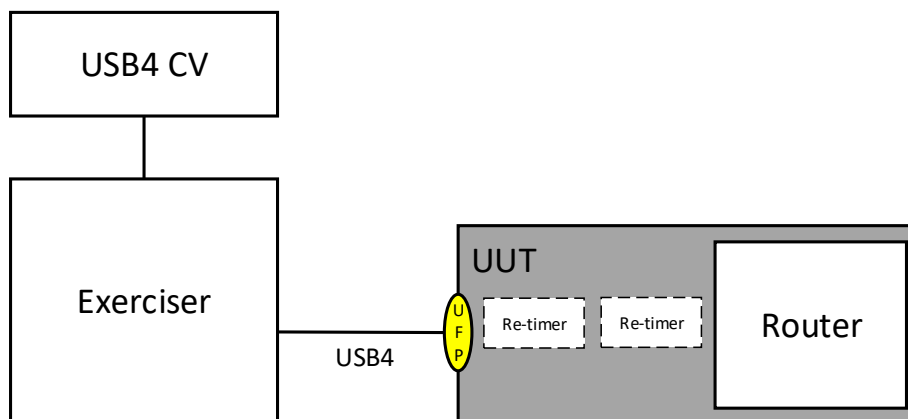
### AN\_DEV\_UFP1

- A KG USB4 Host is connected to the UUT
- USB4 CV is installed on the KG Host System
- A USB4 Analyzer is connected between the UUT and KG USB4 Host



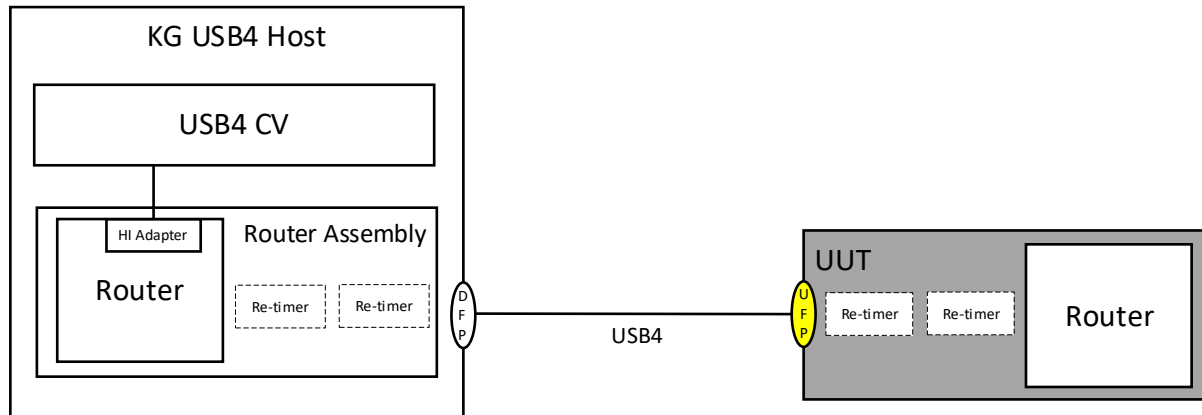
### EX\_DEV\_UFP1

- The Exerciser is connected to the UUT
- Unless specified otherwise, the Exerciser is configured as a USB4 DFP



## DC\_DEV\_UFP1

- A KG USB4 Host is connected to the UUT
- USB4 CV is installed on the KG Host System
- Test steps that require an Analyzer are skipped



## TBT3-Compatibility Mode Test Setups

This section defines the test setups for a Router Assembly that is part of a USB4™ host, hub, or device. The test setups in this section are used for the TBT3-Compatibility Tests.

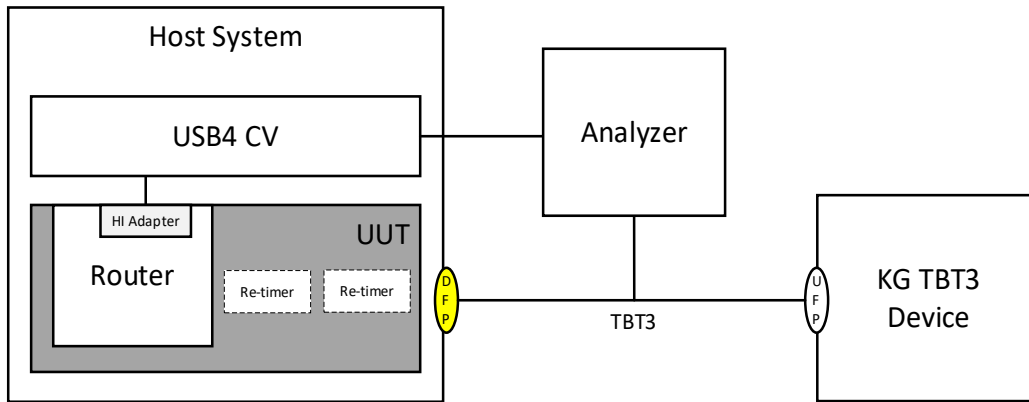
A USB4-Based Dock is tested as a USB4 hub.

### Host

This section describes the test setups for a Router Assembly that is part of a USB4 host. The Port Under Test (PUT) is highlighted in each figure.

## AN\_HOST\_DFP1—TBT3\_01

- A KG USB4 device is connected to the UUT
- USB4 CV is installed on the Host System with the UUT
- A TBT3 Analyzer is connected between the UUT and KG TBT3 Device

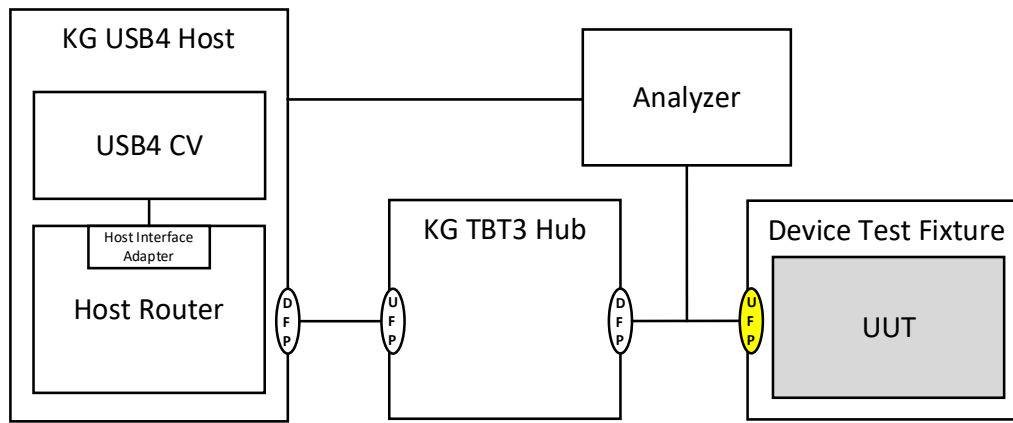


## Hub

This section describes the test setups for a Router Assembly that is part of a USB4 hub. The Port Under Test (PUT) is highlighted in each figure.

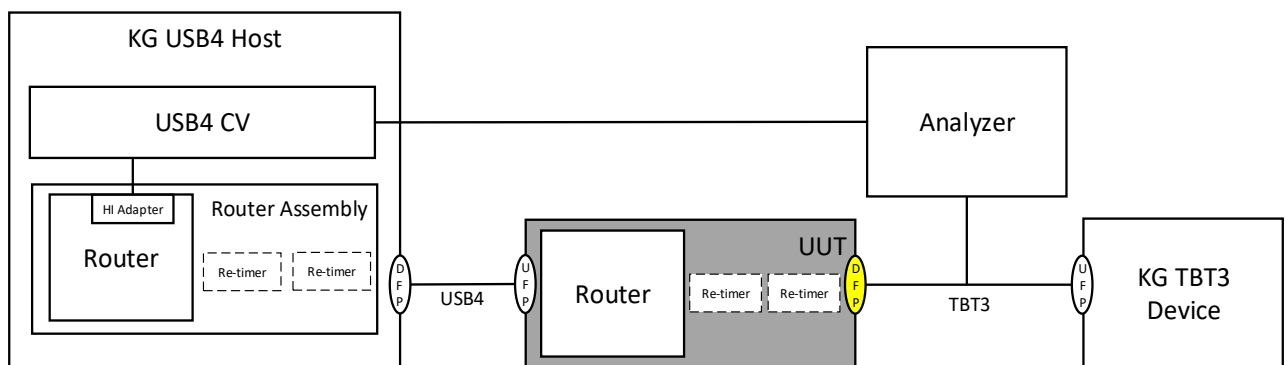
### AN\_HUB\_UFP1—TBT3\_01

- DFP on Compliance Device connects to UFP of a Known Good TBT3 Hub
- DFP on the Known Good TBT3 Hub connects to the UFP of the UUT
- Analyzer is connected between the Known Good TBT3 Hub and the UUT
- USB4 CV runs in TBT3 Compatible Mode



### AN\_HUB\_DFP1—TBT3\_03

- A KG USB4 Host is connected to the UFP of the UUT
- A KG TBT3 Device is connected to the DFP of the UUT
- USB4 CV is installed on the KG Host System
- A USB4 Analyzer is connected between the UUT and KG TBT3 Device

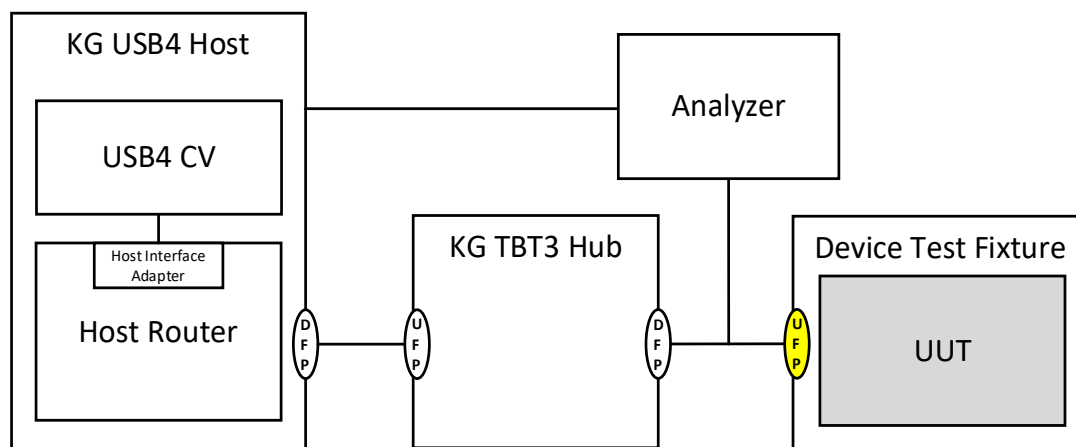


## Peripheral Device

This section describes the test setup for a Router Assembly that is part of a USB4 device. The Port Under Test (PUT) is highlighted in each figure.

### AN\_DEV\_UFP1—TBT3\_01

- DFP on Compliance Device connects to UFP of a Known Good TBT3 Hub
- DFP on the Known Good TBT3 Hub connects to the UFP of the UUT
- Analyzer is connected between the Known Good TBT3 Hub and the UUT
- USB4 CV runs in TBT3 Compatible Mode



## Subroutines

### Router Enumeration Procedure

The following steps are performed to enumerate a Router as a Ver. 1 CM:.

1. Wait for a Hot Plug Event Packet with UPG=0 for Lane 0 and Lane 1
2. Set the *Lock* bit in the Port that detected the connection to 0b
3. Send the Router a Read Request that reads DW0 through DW4.
4. Send the UUT a Write Request that writes the following fields:
  - a. *Connection Manager USB4 Version* = 1.0 (for a USB4 Connection Manager)
  - b. *Connection Manager USB4 Version* = 0.0 (for a TBT3 Connection Manager)
  - c. *Topology ID* = Router TopologyID (assigned per USB4 Specification)
  - d. *Depth* = Router depth (0 for a Host Router, or 1 for a Device Router)
  - e. *Valid* = 1b
5. In each Lane Adapter, set the *Disable Time Sync* bit in the TMU Adapter Configuration Capability to 1b, per Section 7.4.3.1 of the Connection Manager Guide.

The following steps are performed to enumerate a Router as a Ver. 2 CM:

1. (Device Router only) Wait for a Hot Plug Event Packet with UPG=0 for Lane 0 and Lane 1
2. (Device Router only) “Unlock” the DFP that the Router is connected to by writing 0b to the ADP\_CS\_4.Lock bit in the DFP
3. Send the Router a Read Request that reads DW0 through DW4.
4. Send the Router a Write Request that writes the following fields:
  - a. *Connection Manager USB4 Version* = 2.0
  - b. *Topology ID* = Router TopologyID (assigned per USB4 Specification)
  - c. *Depth* = Router depth (0 for a Host Router, 1 or more for a Device Router)
  - d. *Upstream Adapter* = the value read earlier (i.e., value does not change)
  - e. *TopologyID Valid* = 1b
5. Wait 50ms for reception of a Notification Packet with Event Code = ROP\_CMPLT and the Event Info field set to 01h
6. Read the Router Ready bit to verify it is set to 1b
7. Scan all Router Ports and identify each Port’s Adapter Type from the Adapter Type Protocol, Adapter Type Version, and Adapter Type Sub-type fields
8. In each Lane Adapter, set the *Disable Time Sync* bit in the TMU Adapter Configuration Capability to 1b, per Section 7.4.3.1 of the Connection Manager Guide.
9. If supported, enable USB3 GenX tunneling by setting USB3 Tunneling On bit to 1b
10. If supported, enable PCIe tunneling by setting PCIe Tunneling On bit to 1b
11. Set the ROUTER\_CS\_5.Configuration Valid bit to 1b
12. Wait 50ms for reception of a Notification Packet with Event Code = ROP\_CMPLT and the Event Info field set to 02h
13. Read the Configuration Ready bit to verify it is set to 1b

### Lane Bonding Initiation Procedure

The steps in this section are performed whenever a test step calls for Lane bonding to be initiated.

1. Send the UUT a Write Request that writes the following fields:
  - a. *Target Link Width* = 1b
2. Send the Link Partner of the UUT a Write Request that writes the following fields:

- a. *Target Link Width* = 1b
3. Send the Lane 0 Adapter in the DFP (whether it's the UUT or its Link Partner) a Write Request that writes the following fields:
  - a. *Lane Bonding* = 1b
4. Wait for a Hot Plug Packet with UPG=1 for Lane 1

## Configuration Space Reset Procedure

In the PUT, set the following registers to their default values:

1. ROUTER\_CS\_1:
  - a. Depth = 0
2. ROUTER\_CS\_2 = 0
3. ROUTER\_CS\_3 = 0
4. ROUTER\_CS\_4:
  - a. Notification Timeout = 0Ah
  - b. Connection Manager USB4 Version = 0
5. ROUTER\_CS\_5 = 0
6. ROUTER\_CS\_9 to ROUTER\_CS\_26 = 0
7. TMU\_RTR\_CS\_0:
  - a. Freq Measurement Window = 800
  - b. Time Disruption = 0
  - c. Inter-Domain Enable = 0
8. TMU\_RTR\_CS\_3:
  - a. TSPacketInterval = 0
9. TMU\_RTR\_CS\_15:
  - a. FreqAvgConst = 8
  - b. DelayAvgConst = 8
  - c. OffsetAvgConst = 8
  - d. TSInterDomainInterval = 0
  - e. TMU\_RTR\_CS22 to TMU\_RTR\_CS\_25 = 0
10. ADP\_CS\_4:
  - a. Non-Flow Controlled Buffers = 0
11. ADP\_CS\_5 to ADP\_CS\_8 = 0
12. TMU\_ADP\_CS\_3 = 0
13. TMU\_ADP\_6
  - a. Disable Time Sync = 0
14. LANE\_ADP\_CS\_1:
  - a. Target Link Speed = 1100b (if Gen 3 supported)
  - b. Target Link Speed = 1000b (if Gen 3 not supported)
  - c. Target Link Width = 00001b (two Single-Lane Links)
  - d. CL0s Enable = 0b
  - e. CL1 Enable = 0b
  - f. CL2 Enable = 0b
  - g. Lane Disable = 0b
  - h. PM Secondary = 1b
15. LANE\_ADP\_CS\_2 = 0
16. PORT\_CS\_0 to PORT\_CS\_17 = 0
17. PORT\_CS\_19:
  - a. Request RS-FEC Gen 2 = 1b
  - b. Request RS-FEC Gen 3 = 1b
  - c. USB4 Port is Configured = 0b
  - d. USB4 Port is Inter-Domain = 0b
  - e. Enable Wake on Connect = 0b
  - f. Enable Wake on Disconnect = 0b



- g. Enable Wake on USB4 Wake = 1b
- h. Enable Wake on Inter-Domain = 0b
- 18. PATH\_CS\_0 to PATH\_CS\_1 = 0
- 19. Read ADP\_CS\_3 (to clear error fields)

## Router Assembly Reset Procedure

The steps in this section are performed whenever a test calls for a UUT to be reset.

### Host Router

Perform the following steps if the Host Router is a Ver. 1 Router:

1. Teardown any Paths in the RUT
2. Disable, then enable all Transmit and Receive Rings
3. Perform a DFP Reset in each of the Downstream Facing Ports
4. Reset the Host Interface using the Host Interface Reset Register

Perform the following steps if the Host Router is a Ver. 2 Router:

1. Set the Host Router Reset bit in the Host Interface PCIe Memory BAR to 1b
2. Wait for 50ms
3. Poll the Host Router Reset bit for 500ms or until its value is 0b
4. Verify that the Host Router Reset bit is set to 0b within 500ms

### Device Router

Upstream of the UUT in the DFP that is connected to the UUT:

1. Set the *Downstream Port Reset* bit to 1b
2. Read the *Lock* bits for the Lane 0 and Lane 1 Adapters
3. Poll the *Lock* bits until both are 1b
4. Set the Downstream Port Reset bit to 0b

## Router Assembly Connect Procedure

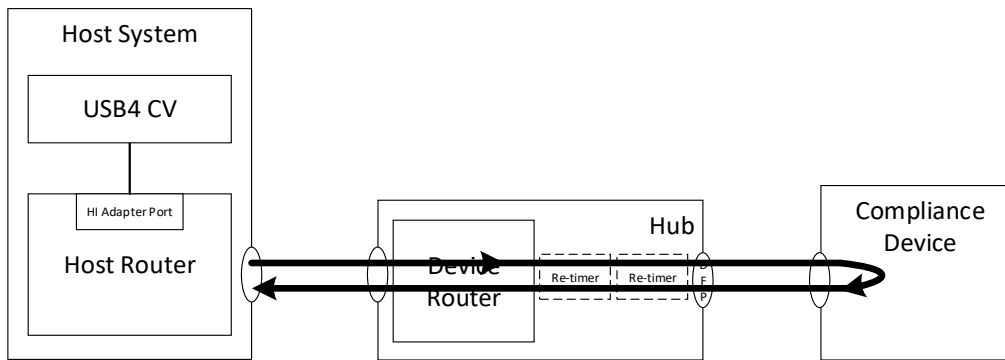
When a test step calls for a Host/Device to be connected, the Analyzer initiates a connect event.

## Router Assembly Disconnect Procedure

When a test step calls for a Host/Device to be disconnected, the Analyzer initiates a disconnect event.

## Loopback Path Setup

A Loopback Path allows USB4 CV to inject traffic into a USB4 fabric by sending itself USB4 Packets using Host-to-Host Tunneling. The USB4 Packets are generated by USB4 CV and routed through the UUT out to the Compliance Device and back through the UUT. The loopback Path uses Ring 1.



The steps in this section are performed whenever a test calls for a loopback path to be setup.

*Note: When Lanes are bonded, only Lane 0 Path Configuration Space needs to be configured.*

#### Part 0 – Configure Adapters Credits fields

Upstream of the UUT, in each Lane Adapter along the loopback Path configure the following:

- If the loopback Path is configured with Flow Control Disabled, set the *Non-Flow Controlled Buffers* field in the Adapter Configuration Space to: *Total Buffers – Path Credits Allocated* for Path 0.
- If the loopback Path is configured with Restricted Shared or Shared flow control, set the *Link Credits Allocated* field in the Adapter Configuration Space to:  $\text{MIN}(\text{Total Buffers} - \text{Path Credits Allocated for Path 0}, 128)$ .

#### Part 1 – Configure the Path Segments

Upstream of the UUT, in each Adapter along the loopback Path starting with the Source Adapter and ending with the Destination Adapter:

1. For all Adapters, configure the HopID/routing table using the following fields in Path Configuration Space:
  - a. *Output Adapter*
  - b. *Output HopID*
  - c. *Priority*
  - d. *Weight*
2. If Adapter is Lane Adapter, set the Flow Control parameters using the following fields in Path Configuration Space:
  - a. *Path Credits Allocated*
  - b. *ESE*
  - c. *ISE*
  - d. *EFC*
  - e. *IFC*
3. Set the *Valid* bit in Path Configuration Space to 1b

#### Part 2 – Enable Loopback

After all Path segments are configured, do the following in each Protocol Adapter along the loopback Path starting with the Source Adapter and ending with the Destination Adapter

4. Set the *Enable* bit in Adapter Configuration Space to 1b

## Loopback Path Teardown

The steps in this section are performed whenever a test calls for a loopback Path to be torn down.

### Part 1 – Disable Loopback

Upstream of the UUT, in each Protocol Adapter along the loopback Path starting with the Destination Adapter and ending with the Source Adapter:

1. Set the *Enable* bit in Adapter Configuration Space to 0b

### Part 2 – Teardown Path Segments

Upstream of the UUT in each Adapter along the loopback Path starting with the Destination Adapter and ending with the Source Adapter:

2. Set the *Valid* bit in Path Configuration Space to 0b
3. Read the *Pending Packets* bit in Path Configuration Space
4. Poll the *Pending Packets* bit until it is 0b
5. Wait tTeardown time

## Initiate Read From SB Register Space

The steps in this section are performed whenever a test calls for a Read Command to be sent.

1. Write to the following fields in the USB4 Port Capability in PUT Configuration Space:
  - a. *Target*
  - b. *Address*
  - c. *Length*
  - d. *WnR* = 0 (Read)
2. Set the *Pending* bit in the USB4 Port Capability in PUT Configuration Space to 1b
3. Poll the *Pending* bit until it is 0b
4. Read the following fields and verify values:
  - a. *No Response* = 0
  - b. *Result Code* = 0 (success)

## Initiate Write to SB Register Space

The steps in this section are performed whenever a test calls for a Write Command to be sent.

1. Write to the following fields in the USB4 Port Capability in PUT Configuration Space:
  - a. *Target*
  - b. *Address*
  - c. *Length*
  - d. *WnR* = 1 (Write)
  - e. *Data DW*
2. Set the *Pending* bit in the USB4 Port Capability in PUT Configuration Space to 1b
3. Poll the *Pending* bit until it is 0b
4. Read the following fields and verify values:
  - a. *No Response* = 0
  - b. *Result Code* = 0 (success)

## USB4 Mode Tests – No Exerciser

The tests in this section are performed in USB4 mode, where all connected Ports negotiate and enter USB4 operation as described in the USB Type-C Specification and the USB PD Specification. The Sideband Channel operates as a USB4 Sideband Channel.

Unless specified otherwise, the tests in this section are performed on all Ports of a UUT. The tests are performed at the highest speed that the UUT supports. Lanes are bonded and RS-FEC is enabled.

Unless otherwise noted, a test will timeout if it takes more than 500ms to go from one step to the next step. It is a test failure if a test step times out.

### Background Checks

The tests in this section verify that the Sideband Channel of the PUT is compliant with the USB4 Specification.

#### Sideband Channel Background Check

This test is performed by the Analyzer in conjunction with all of the Sideband Channel Tests.

1. Parse each LT Transaction and verify that it consists of the following symbols in the following order: (4.1.1.2.1#1)

- a. A DLE symbol (FEh)
- b. A LSE symbol
- c. A CLSE symbol

2. Parse the LSE Symbol in each LT Transaction and verify that:

- a. Bits [7:6] (*StartLT*) are set to 10b (4.1.1.2.1#4)
- b. Bit 5 (*LSELane*) is 0 for an LT\_LRoff Transaction (4.1.1.2.1#3)
- c. Bit 4 is reserved (0b) (1.7#5)
- d. Bit 3 is set to 0b
- e. Bits [2:0] (*LSESymbol*) do not contain reserved values (1.7#1)

*Note: Defined LSESymbol values are 000b (LT\_Fall), 010b (LT\_Resume), 011b (LT\_LRoff), 100b (LT\_SwitchRx2Tx), and 111 (LT\_SwitchAck).*

3. Parse each AT Transaction and verify that it consists of the following symbols in the following order: (4.1.1.2.2#1)

- a. A DLE symbol (FEh)
- b. A STX symbol
- c. No more than 66 Data Symbols (4.1.1.2.2#2)
- d. 2 CRC Symbols (Low and High) with correct CRC (4.1.1.2.4#5, 4.1.1.2.4#6, 4.1.1.2.4#7, 4.1.1.2.4#8, 4.1.1.2.4#9)
- e. A DLE symbol (FEh)
- f. An ETX symbol (40h)

4. For each AT Command:

- a. Parse the STX Symbol and verify that:
  - i. Bits [7:6] (*StartAT*) are 00b (4.1.1.2.2#8)
  - ii. Bit 5 is reserved (0b) (1.7#5)
  - iii. Bit 4 (*Responder*) is 0b (4.1.1.2.2#7)
  - iv. Bit 3 (*Bounce*) is set to 0b (4.1.1.2.2#6)
  - v. Bit 2 (*Recipient*) is 1b (4.1.1.2.2#5)
  - vi. Bit 1 (*ReturnBounce*) is set to 0b (4.1.1.2.2#4)

- b. Parse the Data Symbols and verify that: (4.1.1.3.1#1)
      - i. The REG symbol does not contain the values 2 to 4, 10 to 11, or 128 to 255
      - ii. The LEN symbol does not contain a value greater than 64 (4.1.1.3.1#2)
      - iii. If WnR=0, there is no COMMAND\_DATA
      - iv. If WnR=1b, the COMMAND\_DATA is the same length as in the LEN field
5. For each AT Response:
  - a. Parse the STX Symbol and verify that:
    - i. Bits [7:6] (*StartAT*) are 00b (4.1.1.2.2#8)
    - ii. Bit 5 is reserved (0b) (1.7#5)
    - iii. Bit 4 (*Responder*) is 0b (4.1.1.2.2#7)
    - iv. Bit 3 (*Bounce*) is set to 0b (4.1.1.2.2#6)
    - v. Bit 2 (*Recipient*) is 1b (4.1.1.2.2#5)
    - vi. Bit 1 (*ReturnBounce*) is set to 0b (4.1.1.2.2#4)
  - b. Parse the Data Symbols and verify that: (4.1.1.3.1#2)
    - i. A REG symbol does not contain the values 2 to 4, 10 to 11, or 128 to 255.
    - ii. A LEN symbol does not contain a value greater than 64 (4.1.1.3.1#2)
    - iii. If WnR=0b, RESPONSE\_DATA is the same length as in the LEN field (unless test specifies otherwise)
    - iv. If WnR=1n, RESPONSE\_DATA is 00h (unless test specified otherwise)
  - c. Verify that the value in the LEN field is not greater than 64 (4.1.1.3.1#2)
6. When the PUT receives an AT Command with the Recipient bit set to 1b, verify that the PUT responds with an AT Response (unless the test specifies otherwise). (4.1.1.2.2#9)
7. Parse each Broadcast RT Transaction and verify that it consists of the following symbols in the following order: (4.1.1.2.3.1#1)
  - a. A DLE symbol (FEh)
  - b. A STX symbol
  - c. Two Link Parameters symbols
  - d. 2 CRC Symbols (Low and High) with correct CRC (4.1.1.2.4#5, 4.1.1.2.4#6, 4.1.1.2.4#7, 4.1.1.2.4#8, 4.1.1.2.4#9)
  - e. A DLE symbol (FEh)
  - f. An ETX symbol (40h)
8. Parse the STX Symbol for a Broadcast RT Transaction and verify that:
  - a. If there are no Re-timers on the Link, *Index* = 0 (4.1.1.2.3.1#4)
  - b. If there are Re-timers on the Link, *Index* = the number of On-Board Re-timers in the PUT (see VIF) plus the number of Cable Re-timers between the PUT and the Analyzer (4.1.1.3.1#1rt)
  - c. *CmdNotResp*=1b (4.1.1.2.3.1#5)
9. Parse Byte 2 of a Broadcast RT Transaction and verify that:
  - a. Bits [7:5] are 0 (reserved) (1.7#5)
  - b. Bit 4 (*TBTPCompatibleSpeed*) is 0b (4.1.1.2.3.1#6)
  - c. Bit 3 (*SSCAwaysOn*) is 0b for Gen 4 Link
  - d. Bit 1 (reserved) is 0b (1.7#5)
  - e. Bit 0 (*USB4*) is 1b (4.1.1.2.3.1#7)
10. Parse each Addressed RT Transaction and verify that it consists of the following symbols in the following order: (4.1.1.2.3.2#1)
  - a. A DLE symbol (FEh)
  - b. A STX symbol
  - c. No more than 66 Data Symbols (4.1.1.2.3.2#2)

- d. 2 CRC Symbols (Low and High) with correct CRC (4.1.1.2.4#5, 4.1.1.2.4#6, 4.1.1.2.4#7, 4.1.1.2.4#8, 4.1.1.2.4#9)
  - e. A DLE symbol (FEh)
  - f. An ETX symbol (40h)
11. Parse each RT Command and verify that: (4.1.1.3.1#1)
- a. The REG symbol does not contain the values 2 to 4, 10 to 11, or 128 to 255.
  - b. The LEN symbol does not contain a value greater than 64
  - c. If WnR=0, there is no COMMAND\_DATA
  - d. If WnR=1b, the COMMAND\_DATA is the same length as in the LEN field
12. Parse each RT Response and verify that: (4.1.1.3.1#2)
- a. The REG symbol does not contain the values 2 to 4, 10 to 11, or 128 to 255
  - b. The LEN symbol does not contain a value greater than 64 (4.1.1.3.1#2)
  - c. If WnR=0b, RESPONSE\_DATA is the same length as in the LEN field (unless test specifies otherwise)
  - d. If WnR=1n, RESPONSE\_DATA is 00h (unless test specified otherwise)
13. Verify that the PUT sends an AT Response within tCmdResponse (50ms) of receiving an AT Command. (4.1.1.2.5.1#1)
14. Verify that the PUT sends an Addressed RT Response within tCmdResponse (50ms) of receiving an Addressed RT Command. (4.1.1.2.5.2#1)
15. Verify that PUT did not resend the Write Command or send another AT Command or Addressed RT Command until after the Write Command timed out (4.1.1.2.5#3)
16. Parse each ELT Transaction and verify that it consists of the following symbols in the following order:
- a. A DLE symbol (FEh)
  - b. A ELSE symbol
  - c. A CELSE symbol
17. Parse the ELSE Symbol in each ELT Transaction and verify that:
- a. Bits [7:6] (StartLT) are set to 10b (4.1.1.2.1#4)
  - b. Bit [5:4] (ELTtype) do not contain reserved value
  - c. Bit 3 (ELT) is set to 1b
  - d. Bits [2:0] are reserved (000b)

*Note: Defined ELTtype values are 00b (ELT\_OpDone), and 10b (ELT\_Recovery).*

## Gen 2/Gen 3 Lane 0/Lane 1 Background Check

This test is performed by the Analyzer in conjunction with all of the Lane 0/Lane 1 Tests.

1. Parse each TS1 and TS2 Ordered Set and verify that bits 31:29 (Rsvd) are 0. (4.2.1.3.5#6)
2. When an Adapter transitions to the CL0 state and Lanes are not bonded, verify that the first bytes transmitted after the last TS2 Ordered Set are either a Transport Layer Packet header or an Ordered Set that is not SLOS, TS1, or TS2. (4.4.1#1)
3. When an Adapter transitions to the CL0 state and Lanes are bonded, verify that the first bytes transmitted after the last TS2 Ordered Set are a de-skew Ordered Set followed by either a Transport Layer Packet header, an Idle Packet or any Ordered Set other than SLOS, TS1 or TS2. (4.4.1#2)
4. When operating with a Dual-lane Link, verify that if one Lane transitions to Training State, other Lane also transitions to training state (4.2.2.2#8)

## Gen 4 Lane 0/Lane 1 Background Check

This test is performed by the Analyzer in conjunction with all of the Lane 0/Lane 1 Tests at Gen 4 speed.

1. Parse each Gen 4 TS1-4 and verify that:
  - a. Bits 447:436 are 7E0h
  - b. Bits 431:428 are bitwise complement of bits 435:432
  - c. For TS1-3, bits 427:420 are 0Fh
  - d. For TS4, bits 427:424 are 0h or incrementing counter from 1h to Fh and bits 423:420 are bitwise complement of bits 427:424
  - e. For TS1, bits 419:0 are PRBS11
  - f. For TS2-4, bits 419:0 are PRTS7

## Test Descriptions

### TD 4.001 Invalid Index Test

- A. Purpose
  - Verify that the PUT ignores an Addressed RT Command with an Invalid Index
- B. Asserts:
  - 4.1.1.2.3.2#9
  - 4.1.1.3.2#7rt
- C. Test Setups
  - AN\_HOST\_DFP1/DC\_HOST\_DFP1 (Host)
  - AN\_DEV\_UFP1/DC\_DEV\_UFP1 (Device)
  - AN\_HUB\_UFP1/DC\_HUB\_UFP1 (Hub UFP)
  - AN\_HUB\_DFP1/DC\_HUB\_DFP1 (Hub DFP)
- D. Background Check:
  - Sideband Channel Background Check (if using an Analyzer)
- E. Procedure:

USB4 CV performs the following steps:

1. Start Analyzer (if using an Analyzer)
2. Reset UUT
3. Enumerate UUT Router
4. Initiate Lane Bonding
5. Tell the Link Partner to send the PUT an Addressed RT Transaction by writing the following to PORT\_CS\_1 of the Link Partner:
  - a. *WnR* = 0b (Read Command)
  - b. *Address* = Register 9 (Metadata)
  - c. *Retimer Index* = 0
  - d. *Target* = 010b (re-timer)
  - e. *Length* = 4
6. Wait for the Read Response from the PUT
7. Record the values in the RESPONSE\_DATA in the Read Response
8. Tell the Link Partner to send an Addressed RT Transaction to the PUT by writing the following to PORT\_CS\_1 of the Link Partner:
  - a. *WnR* = 0b (Read Command)
  - b. *Address* = Register 9 (Metadata)
  - c. *Retimer Index* = 7
  - d. *Target* = 010b (re-timer)
  - e. *Length* = 4
9. Wait for the Transaction to timeout
10. Verify that the PUT did not send a Read Response (4.1.1.2.3.2#9, 4.1.1.3.2#7rt)
  - a. Read the *No Response* bit in PORT\_CS\_1
  - b. Verify that the *No Response* bit is 1b
11. Tell the Link Partner to send an Addressed RT Transaction to the PUT by writing the following to PORT\_CS\_1 and PORT\_CS\_2 of the Link Partner:
  - a. *WnR* = 1b (Write Command)
  - b. *Address* = Register 9 (Metadata)
  - c. *Retime Index* = 7



- d. *Target* = 010b (re-timer)
  - e. *Length* = 4
  - f. *Command Data* = FFFF FFFFh
- 12. Wait for the Transaction to timeout
- 13. Verify that the PUT did not send a Write Response (4.1.1.2.3.2#9, 4.1.1.3.2#7rt)
  - a. Read the *No Response* bit in PORT\_CS\_1
  - b. Verify that the *No Response* bit is 1b
- 14. Tell the Link Partner to send the PUT an Addressed RT Transaction by writing the following to PORT\_CS\_1 of the Link Partner:
  - f. *WnR* = 0b (Read Command)
  - g. *Address* = Register 9 (Metadata)
  - h. *Retimer Index* = 0
  - i. *Target* = 010b (re-timer)
  - j. *Length* = 4
- 15. Wait for the Read Response from the PUT
- 16. Verify that the contents of Register 9 match what was read from Register 9 in Step 5 (i.e. the previous Read and Write Commands had no effect) (4.1.1.2.3.2#9, 4.1.1.3.2#7rt)
- 17. Stop Analyzer (if using an Analyzer)

#### TD 4.002 FEh Data Symbol Test

A. Purpose:

- Verify that the PUT correctly handles Transactions with FEh data symbols

B. Asserts:

- 4.1.1.2.4#3, 4.1.1.2.4#4

C. Test Setups

- AN\_HOST\_DFP1/DC\_HOST\_DFP1 (Host)
- AN\_DEV\_UFP1/DC\_DEV\_UFP1 (Device)
- AN\_HUB\_UFP1/ DC\_HUB\_UFP1 (Hub UFP)
- AN\_HUB\_DFP1/ DC\_HUB\_DFP1 (Hub DFP)

D. Repetitions:

- Repeat with AT Transactions
- Repeat with Addressed RT Transactions with the following:
  - *Index* = 0
  - *Index* = First On-Board Re-timer (if present)
  - *Index* = Second On-Board Re-timer (if present)

E. Background Check:

- Sideband Channel Background Check (if using an Analyzer)

F. Procedure:

USB4 CV performs the following steps:

1. Start Analyzer (if using an Analyzer)
2. Reset UUT
3. Enumerate UUT Router
4. Initiate Lane Bonding
5. Tell the Link Partner to send the PUT a Write Command with the following:
  - a. *Target* = Register 9 (Metadata)
  - b. *Length* = 4
  - c. *Command Data* = FE 00 FE 00h
  - d. Insert a leading FEh before each FEh data symbol
6. Verify that the PUT sends a Write Response with no error (4.1.1.2.4#4)
7. Tell the Link Partner to send the PUT a Read Command with the following:
  - a. *Target* = Register 9 (Metadata)
  - b. *Length* = 4
8. Wait for the AT Read Response from the PUT
9. Verify that the contents of Register 9 are the same as previously written (FE 00 FE 00h) (4.1.1.2.4#3)
10. Stop Analyzer (if using an Analyzer)

## TD 4.003 SB Register Write Error Test

### A. Purpose:

- Verify that the PUT correctly handles Write Request error cases

### B. Asserts:

- 4.1.1.3.1#12-16
- 4.1.1.3.3#1

### C. Test Setups

- AN\_HOST\_DFP1/ DC\_HOST\_DFP1 (Host)
- AN\_DEV\_UFP1/ AN\_DEV\_UFP1 (Device)
- AN\_HUB\_UFP1/ DC\_HUB\_UFP1 (Hub UFP)
- AN\_HUB\_DFP1/ DC\_HUB\_DFP1 (Hub DFP)

### D. Repetitions:

- Repeat with AT Transactions
- Repeat with Addressed RT Transactions with the following:
  - *Index* = 0
  - *Index* = First On-Board Re-timer (if present)
  - *Index* = Second On-Board Re-timer (if present)

### E. Background Check:

- Sideband Channel Background Check (if using an Analyzer)

### F. Procedure:

USB4 CV does the following:

#### Part 0 - Setup

1. Start Analyzer (if using an Analyzer)
2. Reset UUT
3. Enumerate UUT Router
4. Initiate Lane Bonding

#### Part 1 – Invalid Target

5. Tell the Link Partner to send the PUT a Write Command that targets an undefined register
6. Verify that the PUT responds with a Write Response with:
  - a. *LEN* = 0
  - b. *RESPONSE\_DATA* = 01h (error Result Code) (4.1.1.3.1#12)

#### Part 2 – Write Length Mismatch

7. Tell the Link Partner to send the PUT a Read Command with *Target* = Register 9 (Metadata)
8. Record the *RESPONSE\_DATA* returned by the PUT
9. Tell the Link Partner to send the PUT a Write Command with:
  - a. *Target* = Register 9 (Metadata)
  - b. *COMMAND\_DATA* is 8 bytes
  - c. *LEN* = 9

10. Verify that the PUT responds with a Write Response with:
  - a. LEN = 0 (4.1.1.3.1#13)
  - b. RESPONSE\_DATA = 01h (error Result Code) (4.1.1.3.1#13)
11. Tell the Link Partner to send the PUT a Read Command with *Target* = Register 9 (Metadata)
12. Verify that the RESPONSE\_DATA in the Read Response from the PUT is the same as the RESPONSE\_DATA recorded in Step 8 (4.1.1.3.1#13)

#### Part 3 – Write to Read-Only Register

13. Tell the Link Partner to send the PUT a Read Command with *Target* = Register 0 (Vendor ID)
14. Record the RESPONSE\_DATA returned by the PUT
15. Tell the Link Partner to send the PUT a Write Command with *Target* = Register 0 (Vendor ID)
16. Verify that the PUT responds with a Write Response with:
  - a. LEN = 0 (4.1.1.3.1#14)
  - b. RESPONSE\_DATA = 01h (error Result Code) (4.1.1.3.1#14)
17. Tell the Link Partner to send the PUT a Read Command with *Target* = Register 0 (Vendor ID)
18. Verify that the RESPONSE\_DATA in the Read Response from the PUT is the same as the RESPONSE\_DATA recorded in Step 14 (4.1.1.3.3#1)

#### Part 4 – Long Write

19. Tell the Link Partner to send the PUT a Read Command with *Target* = Register 9 (Metadata)
20. Record the RESPONSE\_DATA returned by the PUT
21. Tell the Link Partner to send the PUT a Write Command with:
  - a. *Target* = Register 9 (Metadata)
  - b. LEN = 5
22. Verify that the PUT responds with a Write Response with:
  - a. LEN = 0 (4.1.1.3.1#15)
  - b. RESPONSE\_DATA = 01h (error Result Code) (4.1.1.3.1#15)
23. Tell the Link Partner to send the PUT a Read Command with *Target* = Register 9 (Metadata)
24. Verify that the RESPONSE\_DATA in the Read Response from the PUT is the same as the RESPONSE\_DATA recorded in Step 20 (4.1.1.3.1#15)

#### Part 5 – Short Write

25. Tell the Link Partner to send the PUT a Read Command with *Target* = Register 9 (Metadata)
26. Record the RESPONSE\_DATA returned by the PUT
27. Tell the Link Partner to send the PUT a Write Command with:
  - a. *Target* = Register 9 (Metadata)
  - b. LEN = 3
  - c. COMMAND\_DATA = FF FF FFh
28. Verify that the PUT responds with a Write Response with:
  - a. RESPONSE\_DATA = 00h (Success Result Code) (4.1.1.3.1#16)
29. Tell the Link Partner to send the PUT a Read Command with *Target* = Register 9 (Metadata)
30. Verify that the MSB in the RESPONSE\_DATA in the Read Response from the PUT is the same as the MSB in the RESPONSE\_DATA recorded in Step 26 (4.1.1.3.1#16)
31. Verify that the remaining bytes in the RESPONSE\_DATA are FFFh (4.1.1.3.1#16)
32. Stop Analyzer (if using an Analyzer)

TD 4.004 [Moved](#)

Moved to TD 4.004 Command Timeout Test (Exerciser Required)

## TD 4.005 Lane Initialization Phase Test

*Note: This test is performed simultaneously for both the Lane 0 Adapter and the Lane 1 Adapter of the Port being tested.*

### A. Purpose:

- Verify that the PUT behaves correctly during Lane Initialization
- Verify that SB Register Space format, fields, and values are correct
- Verify maximum sized read (64 bytes) from SB Register space

### B. Asserts:

- 4.1.1.2.3.1#4, 4.1.1.2.3.1#8-9
- 4.1.1.3.1#1rt, 4.1.1.3.1#2rt, 4.1.1.3.1#5rt
- 4.1.1.3.3#6, 4.1.1.3.3#8-13, 4.1.1.3.3#13-15, 4.1.1.3.3#23-27
- 4.1.2.2#1-2
- 4.1.2.2#1rt
- 4.1.2.3#1-2, 4.1.2.3#4-8, 4.1.2.3#11, 4.1.2.3#14, 4.1.2.3#17
- 4.1.2.4#1-5
- 4.1.2.5#2, 4.1.2.5#4, 4.1.2.5#5
- 4.1.2.5#2rt, 4.1.2.5#7rt-9rt
- 4.1.2.5.1.1#2-7
- 4.1.2.5.1.2#2, 4.1.2.5.1.2#3, 4.1.2.5.1.2#5-7, 4.1.2.5.1.2#9, 4.1.2.5.1.2#11-12
- 4.2.1.4.1#1
- 4.2.2.2#1, 4.2.2.2#3-5

### C. Test Setups

- AN\_HOST\_DFP1/ DC\_HOST\_DFP1 (Host)
- AN\_DEV\_UFP1/ DC\_DEV\_UFP1 (Device)
- AN\_HUB\_UFP1/ DC\_HUB\_UFP1 (Hub UFP)
- AN\_HUB\_DFP1/ DC\_HUB\_DFP1 (Hub DFP)

### D. Repetitions:

- Repeat at all supported Link speeds:
  - For 20G: Gen 2x2
  - For 40G: Gen 2x2, Gen 3x1, Gen 3x2
  - For 80G: Gen 2x2, Gen 3x1, Gen 3x2, Gen 4x2
  - For 120/40G: Gen 4 3 Tx, Gen 4 3 Rx – if UFP supports default Asymmetric
- Repeat with:
  - RS-FEC on
  - RS-FEC off (Gen 2 and Gen 3 only)

### E. Background Check:

- Sideband Channel Background Check (if using an Analyzer)

### F. Procedure:

USB4 CV performs the following steps:

#### Part 0 – Setup

1. Start Analyzer (if using an Analyzer)
2. Reset UUT
3. Enumerate UUT Router

4. Set the Link speed in the DFP:
  - a. For Gen 2x2:
    - i. *Target Link Speed* = Gen 2
    - ii. *Lane Disable (Lane 0)* = 0b
    - iii. *Lane Disable (Lane 1)* = 0b
  - b. For Gen 3x1:
    - i. *Target Link Speed* = Gen 3
    - ii. *Lane Disable (Lane 0)* = 0b
    - iii. *Lane Disable (Lane 1)* = 1b
  - c. For Gen 3x2:
    - i. *Target Link Speed* = Gen 3
    - ii. *Lane Disable (Lane 0)* = 0b
    - iii. *Lane Disable (Lane 1)* = 0b
  - d. For Gen 4x2:
    - i. *Target Link Speed* = Gen 4
    - ii. *Lane Disable (Lane 0)* = 0b
    - iii. *Lane Disable (Lane 1)* = 0b
    - iv. *Request Asymmetric Tx* = 0b
    - v. *Request Asymmetric Rx* = 0b
  - e. For Gen 4 3 Tx: (if UFP supports default Asymmetric 3 Rx)
    - i. *Target Link Speed* = Gen 4
    - ii. *Lane Disable (Lane 0)* = 0b
    - iii. *Lane Disable (Lane 1)* = 0b
    - iv. *Request Asymmetric Tx* = 1b
    - v. *Request Asymmetric Rx* = 0b
  - f. For Gen 4 3 Rx: (if UFP supports default Asymmetric 3 Tx)
    - i. *Target Link Speed* = Gen 4
    - ii. *Lane Disable (Lane 0)* = 0b
    - iii. *Lane Disable (Lane 1)* = 0b
    - iv. *Request Asymmetric Tx* = 0b
    - v. *Request Asymmetric Rx* = 1b
5. Set RS-FEC on/off in the DFP:
  - a. Gen 2 – RS-FEC is on
    - i. *Request RS-FEC Gen 2* = 1b
  - b. Gen 2 – RS-FEC is off
    - i. *Request RS-FEC Gen 2* = 0b
  - c. Gen 3 – RS-FEC is on
    - i. *Request RS-FEC Gen 3* = 1b
  - d. Gen 3 – RS-FEC is off
    - i. *Request RS-FEC Gen 3* = 0b

#### Part 1 – Phases 1 and 2

6. Disconnect then connect the PUT by performing a Downstream Port Reset (DPR)
  - a. If the PUT is a UFP, perform the DPR on the DFP connected to the PUT
  - b. If the PUT is a DFP, perform the DPR on the PUT
7. Verify that SBTX goes high on the UUT for at least tConnectRx time (4.1.2.2#1, 4.1.2.2#2, 4.1.2.2#1rt)

#### Part 2 – Phase 3

8. Verify that the PUT sends one or more AT Transactions to read the Link Configuration Register (Register 12) of the Link Partner (4.1.2.3#1)

9. Verify that the PUT avoids a tATTimeout delay by sending one or more additional AT Transactions (4.1.2.3#2)

#### Part 3 – Phase 4

10. Verify that the PUT sends a Broadcast RT Transaction every tLaneParams (4.1.2.4#1, 4.1.1.3.1#2rt)
11. Record the value in the Re-timer Index field of the Broadcast Transaction

*Note: The Re-Timer Index is 0 when a Router first creates and sends a Broadcast Transaction. It is then incremented by 1 by each re-timer on the Link. The number of On-Board Re-timers on the PUT is equal to the Re-timer Index field minus the number of any additional Cable Re-timers and On-Board Re-timers the Broadcast RT Transaction traverses before being captured.*

12. Verify that the Re-timer Index indicates the correct number of On Board Re-timers on the PUT, as indicated in the USB4\_Num\_Retimers field in the VIF (4.1.1.2.3.1#4, 4.1.1.3.1#1rt)
13. Verify that the PUT sends Broadcast RT Transactions until all of the following are true: (4.1.2.4#2)
  - a. At least tLTPHase4 time has passed from completion of Phase 2
  - b. The PUT sent at least two Broadcast RT Transactions
14. For each Broadcast RT Transaction from the PUT, verify: (4.1.2.4#1)
  - a. TBT3-Compatible Speed = 0b
  - b. If Link is configured with RS-FEC encoding on, RS\_FEC = 1b
  - c. If Link is configured with RS-FEC encoding off, RS\_FEC = 0b
  - d. USB4 bit = 1b
  - e. If Link is configured for Gen 2 speed, Selected Gen = 0001b
  - f. If Link is configured for Gen 3 speed, Selected Gen = 0010b
  - g. If Link is configured for Gen 4 speed, Selected Gen = 0100b
  - h. If Link is Symmetric, Enable3Tx and Enable3Rx = 0b.
  - i. If Link is Asymmetric 3 Tx, Enable3Tx = 1b and Enable3Rx = 0b
  - j. If Link is Asymmetric 3 Rx, Enable3Tx = 0b and Enable3Rx = 1b
  - k. If Link is configured for x1, Lane1Enabled = 0b (4.1.1.2.3.1#8)
  - l. If Link is configured for x2, Lane1Enabled = 1b (4.1.1.2.3.1#8)
  - m. Lane0Enabled = 1b (4.1.1.2.3.1#9)
  - n. If PUT has On-Board Re-timers or Link is Gen 4, SSCAlwaysOn is 0b (4.1.1.3.1#5rt)
15. If the Link is Gen 2 or Gen 3:
  - a. Verify that the PUT sends SLOS (4.1.2.4#3)
  - b. Verify that the PUT sends an LT\_Resume Transaction with LSELane field = 0b (4.1.2.4#4, 4.1.2.4#5)
  - c. If Link is configured for x2, verify that the PUT sends an LT\_Resume Transaction with LSELane field = 1b (4.1.2.4#4, 4.1.2.4#5)
  - d. Wait for the Link Partner to send the PUT an Addressed RT Transaction with:
    - i. Read Command
    - ii. Index = 0
    - iii. Target = Register 13 (TxFFE)
  - e. (if using an Analyzer) In the Read Response from the PUT parse the RESPONSE\_DATA and verify that:
    - i. Tx Active (Lane 0) = 1b (4.1.2.4#4)
    - ii. If Link is configured for x1, Tx Active (Lane 1) = 0b (4.1.2.4#4)
    - iii. If Link is configured for x2, Tx Active (Lane 1) = 1b (4.1.2.4#4)
    - iv. Clock Switch Done = 0b (4.1.2.5#7rt)
16. If the Link is Gen 4:
  - a. Verify that PUT sends LFPS



- b. Verify that after PUT receives LFPS it moves to Electrical Idle for tPreData and then sends Gen 4 TS1.1
- c. Wait for the Link Partner to send the PUT an Addressed RT Transaction with:
  - i. Write Command
  - ii. Index = 0
  - iii. Target = Register 14 (Gen 4 TxFFE)

#### Part 4 – Phase 5

*Note: In this test, a Read Command is an Addressed RT Transaction with the CmdNotResp bit in the STX Symbol set to 1b and the WnR bit in the Data Symbol set to 0b. A Read Response is an Addressed RT Transaction with the CmdNotResp bit in the STX Symbol set to 0b and the WnR bit in the Data Symbol set to 0b. A Write Command is an Addressed RT Transaction with the CmdNotResp bit in the STX Symbol set to 1b and the WnR bit in the Data Symbol set to 1b. A Write Response is an Addressed RT Transaction with the CmdNotResp bit in the STX Symbol set to 0b and the WnR bit in the Data Symbol set to 1b.*

*Note: For Gen 2 and Gen 3 Speeds: for Lane 0, the Rx Status & TxFFE Request byte is Byte 0 in Register 13 and the Tx Status byte is Byte 2 in Register 13. For Lane 1, the Rx Status & TxFFE Request byte is Byte 1 in Register 13 and the Tx Status byte is Byte 3 in Register 13. The bytes for Lane 0 and Lane 1 may be accessed in a single Transaction (e.g. one Read Request that reads all 4 bytes of Register 13) or they may be accessed in separate Transactions.*

*Note: In Gen 4 Link, the Gen 4 Partner Rx Status & TxFFE Request bytes are Bytes 0-3 (depends on the Link properties) in Register 14 and the Gen 4 Partner Tx Status bytes are Bytes 1-3 (depends on the Link properties) in Register 14. See Table 4-20 in the USB4 spec for more details. All the bytes may be accessed in a single Transaction (e.g. one Write Request that writes all 4 bytes of Register 14) or they may be accessed in separate Transactions.*

If the Link is Gen 2/3:

17. (if using an Analyzer) To test the PUT Transmitter, parse the trace from the Analyzer and do the following for both Lane 0 and Lane 1:
  - a. Verify that the PUT sends Read Command with: (4.1.2.5#2, 4.1.2.5#2rt)
    - i. REG = 13 (TxFFE Register) (4.1.2.5.1.1#2)
    - ii. LEN >= 1 (includes Rx Status & TxFFE Request byte) (4.1.2.5.1.1#2)
    - iii. Index = 0b (4.1.2.5#2)
    - iv. If this is a repeated Read Command (i.e. the New Request field was 0b in the last received Read Response), verify that the Read Command was sent within tPollTXFFE time after the PUT received the previous Read Response for the same Lane (4.1.2.5.1.1#3)
  - b. In the Read Response from the Link Partner, parse the Rx Status & TxFFE Request byte:
    - i. If Rx Locked = 1b, TxFFE negotiation is complete, go to Step 18a
    - ii. If New Request = 0b, repeat Step 17a and continue test flow from there
    - iii. If New Request = 1b, continue to the next step
  - c. In the Read Response from the Link Partner, parse the Rx Status & TxFFE Request byte and record the value in the TxFFE Request field.
  - d. Look for a Read Command from the Link Partner that targets the Tx Status byte of the PUT and a Read Response from the PUT that contains the Tx Status byte.
  - e. In the Read Response from the PUT, parse the Tx Status byte of the PUT:
    - i. If Request Done = 0b, repeat Step 17d and continue the test flow from there

- ii. If *Request Done* = 1b, verify that the *TxFE Setting* field matches the *TxFE Request* value recorded in Step 17c (4.1.2.5.1.1#4, 4.1.2.5.1.1#5)
  - f. Verify that the PUT sends a Read Command with:
    - i. *REG* = 13 (TxFFE Register) (4.1.2.5.1.1#6)
    - ii. *LEN* >= 1 (includes *Rx Status* & *TxFE Request* byte) (4.1.2.5.1.1#6)
    - iii. *Index* = 0b (4.1.2.5#2)
    - iv. If this is a repeated Read Command (i.e. the *New Request* field was 1b in the last received Read Response), verify that the Read Command was sent within tPollTXFFE time after the PUT received the previous Read Response for the same Lane (4.1.2.5.1.1#7)
  - g. In the Read Response from the Link Partner, parse the *Rx Status* & *TxFE Request* byte:
    - i. If *New Request* = 1b, repeat Step 17f and continue test flow from there
    - ii. If *New Request* = 0b, continue to the next step
    - iii. If *Rx Locked* = 0b, repeat Step 17a and continue test flow from there
    - iv. If *Rx Locked* = 1b, TxFFE negotiation is complete, go to the next step
18. (if using an Analyzer) To test the PUT Receiver, parse the trace from the Analyzer and do the following for both Lane 0 and Lane 1:
- a. Verify that the PUT sends a Read Command with: (4.1.2.5#4)
    - i. *REG* = 13 (TxFFE Register) (4.1.2.5.1.2#2)
    - ii. *LEN* >= 3 (includes *Tx Status* byte) (4.1.2.5.1.2#2)
    - iii. *Index* = 0b (4.1.2.5#4)
    - iv. If this is a repeated Read Command (i.e. the *Tx Active* bit was 0b in the last received Read Response), verify that the Read Command was sent within tPollTXFFE time after the PUT received the previous Read Response for the same Lane(4.1.2.5.1.2#3)
  - b. In the Read Response from the Link Partner, parse the *TX Status* byte:
    - i. If *Tx Active* = 0b, repeat Step 18a and continue test flow from there
    - ii. If *Tx Active* = 1b, continue to the next step
  - c. Look for a Read Command from the Link Partner that targets the *Tx Status* byte of the PUT and a Read Response from the PUT that contains the *Tx Status* byte.
  - d. In the Read Response from the PUT, parse the *Tx Status* byte:
    - i. If *Rx Locked* = 1b, TxFFE negotiation is complete, end Step 18
    - ii. Else if *New Request* = 0b, return to Step 18c.
  - e. Else if *New Request* = 1b, continue to the next step. Verify that the PUT sends a Read Command with:
    - i. *REG* = 13 (TxFFE Register) (4.1.2.5.1.2#7)
    - ii. *LEN* >= 3 (includes *Tx Status* byte) (4.1.2.5.1.2#7)
    - iii. *Index* = 0b (4.1.2.5#4)
    - iv. If this is a repeated Read Command (i.e. the *Tx Active* bit was 0b or the *Request Done* was 0b in the last received Read Response), verify that the Read Command was sent within tPollTXFFE time after the PUT received the previous Read Response for the same Lane (4.1.2.5.1.2#9)
  - f. In the Read Response from the Link Partner, parse the *TX Status* byte:
    - i. If *TX Active* = 0b or *Request Done* = 0b, repeat Step 18e and continue test flow from there
    - ii. If *TX Active* = 1b and *Request Done* = 1b, continue to the next step
  - g. Look for a Read Command from the Link Partner that targets the *Tx Status* byte of the PUT and a Read Response from the PUT that contains the *Tx Status* byte.
  - h. In the Read Response from the PUT, parse the *Tx Status* byte and verify that:
    - i. *New Request* = 0b (4.1.2.5.1.2#11)
  - i. Verify that the PUT sends a Read Command with:
    - i. *REG* = 13 (TxFFE Register) (4.1.2.5.1.2#12)
    - ii. *LEN* >= 3 (includes *Tx Status* byte) (4.1.2.5.1.2#12)
    - iii. *Index* = 0b (4.1.2.5#4)

- iv. If this is a repeated Read Command (i.e. the *Tx Active* bit was 0b or the *Request Done* was 0b in the last received Read Response), verify that the Read Command was sent within tPollTXFFE time after the PUT received the previous Read Response for the same Lane (4.1.2.5.1.2#14)
- j. In the Read Response from the Link Partner, parse the *TX Status* byte:
  - i. If *TX Active* = 1b and *Request Done* = 0b, repeat Step 18bc and continue test flow from there
  - ii. If *TX Active* = 0b or *Request Done* = 1b, repeat Step 18i and continue test flow from there
- 19. If PUT contains two On-Board Re-timers:
  - a. When the PUT stops sending CL\_WAKE1.X:
    - i. Read the *Clock Switch Done* bit and verify that it is 1b (4.1.2.5#8rt)
    - ii. Verify that the PUT sends CL\_WAKE1.(X+1)
    - iii. When the PUT stops sending CL\_WAKE1.(X+1), verify that it sends SLOS
- 20. If PUT contains one On-Board Re-timer:
  - a. When the PUT stops sending CL\_WAKE1.X:
    - i. Read the *Clock Switch Done* bit and verify that it is 1b (4.1.2.5#8rt)
    - ii. Verify that the PUT sends SLOS

If the Link is Gen 4:

- 21. To test the PUT Transmitter, parse the trace from the Analyzer and do the following for all enabled transmitters:
  - a. Verify that the PUT sends Write Command with:
    - i. REG = 14 (Gen 4 TxFFE Register)
    - ii. LEN >= 2 (includes Gen 4 Partner Tx Status byte) (4.1.2.5.1.1#2)
    - iii. Index = 0b (4.1.2.5#2)
    - iv. If Start TxFFE = 0b, repeat Step 21a and continue test flow from there.
    - v. If Start TxFFE = 1b, continue to next step.
  - b. In the Write Command from the Link Partner, parse the Gen 4 Partner Rx Status & TxFFE Request byte:
    - i. If New Request = 0b, repeat Step 21b and continue test flow from there
    - ii. If New Request = 1b, continue to the next step
  - c. In the Write Command from the Link Partner, parse the Gen 4 Link Partner Rx Status & TxFFE Request byte and record the value in the Gen 4 TxFFE Request field.
  - d. In the Write Command from the PUT, parse the Gen 4 Link Partner Tx Status byte of the PUT:
    - i. If Request Done = 0b, repeat Step 21d and continue the test flow from there
    - ii. If Request Done = 1b, verify that the Gen 4 TxFFE Setting field matches the Gen 4 TxFFE Request value recorded in Step 21c
    - iii. Verify that Request Done was set within tTxFFEResponse from setting the New Request
  - e. In the Write Command from the Link Partner, parse the Gen 4 Partner Rx Status & TxFFE Request byte:
    - i. If New Request = 1b, repeat Step 21e and continue test flow from there
    - ii. If New Request = 0b, continue to the next step.
  - f. In the Write Command from the PUT, parse the Gen 4 Link Partner Tx Status byte of the PUT:
    - i. If Request Done = 1b, repeat Step 21f and continue the test flow from there
    - ii. If Request Done = 0b, verify that Request Done was cleared within tTxFFEResponse from clearing the New Request, go to step 21b and continue the test from there

22. To test the PUT Receiver, parse the trace from the Analyzer and do the following for all enabled receivers:
  - a. Verify that the Link Partner sends Write Command with: (4.1.2.5#2, 4.1.2.5#2rt)
    - i. REG = 14 (Gen 4 TxFFE Register) (4.1.2.5.1.1#2)
    - ii. LEN  $\geq$  2 (includes Gen 4 Partner Tx Status byte) (4.1.2.5.1.1#2)
    - iii. Index = 0b (4.1.2.5#2)
    - iv. If Start TxFFE = 0b, repeat Step 22a and continue test flow from there.
    - v. If Start TxFFE = 1b, continue to next step.
  - b. In the Write Command from the PUT, parse the Gen 4 Partner Rx Status & TxFFE Request byte:
    - i. If New Request = 0b, repeat Step 22b and continue test flow from there
    - ii. If New Request = 1b, continue to the next step
  - c. In the Write Command from the PUT, parse the Gen 4 Link Partner Rx Status & TxFFE Request byte and record the value in the Gen 4 TxFFE Request field.
  - d. In the Write Command from the Link Partner, parse the Gen 4 Link Partner Tx Status byte of the PUT:
    - i. If Request Done = 0b, repeat Step 22d and continue the test flow from there
    - ii. If Request Done = 1b, verify that the Gen 4 TxFFE Setting field matches the Gen 4 TxFFE Request value recorded in Step 22c (4.1.2.5.1.1#4, 4.1.2.5.1.1#5)
  - e. In the Write Command from the PUT, parse the Gen 4 Partner Rx Status & TxFFE Request byte:
    - i. If New Request = 1b, repeat Step 22e and continue test flow from there
    - ii. If New Request = 0b, continue to the next step.
  - f. In the Write Command from the Link Partner, parse the Gen 4 Link Partner Tx Status byte of the PUT:
    - i. If Request Done = 1b, repeat Step 22f and continue the test flow from there
    - ii. If Request Done = 0b, go to step 22b and continue the test from there
23. When Receiver of the Link Partner is ready to transition to PAM3 (sending Gen 4 TS1.2) and the receiver of the PUT is ready to transition to PAM3 (sending Gen 4 TS1.2), verify that the PUT sends Gen 4 TS2.3. Verify that the transition happens within tGen4TS1 time.
24. If PUT contains On-Board Re-timer(s):
  - a. When Receiver of the Link Partner has finished TxFFE (sending Gen 4 TS2.4) and the receiver of the PUT has finished TxFFE (sending Gen 4 TS2.4), verify that the PUT sends Gen 4 TS2.clksw within margin of tPreClkSw and tSwitchNoSSC. Verify that the transition happens within tGen4TS2 time.
25. Else:
  - a. When Receiver of the Link Partner has finished TxFFE (sending Gen 4 TS2.4) and the receiver of the PUT has finished TxFFE (sending Gen 4 TS2.4), verify that the PUT sends Gen 4 TS3.5. Verify that the transition happens within tGen4TS2 time.

#### Part 5 – SB Register Space Verification

26. Wait for a Hot Plug Event Packet with UPG=0b from the PUT (to indicate that Lane Initialization is complete)
27. Enumerate the UUT Router
28. Read the SB Registers Spaces of the PUT:
  - a. Send AT Transactions to read all defined registers in the SB Register Space of the PUT
  - b. Send Addressed RT Transactions to read all defined registers in the SB Register Space of all On-Board Re-timer Ports
29. Verify the following for each SB Register Space:
  - a. For Register 0 (Vendor ID):

- i. Vendor ID Low field matches the Vendor ID field in Router Configuration Space (4.1.1.3.3#8)
  - ii. Vendor ID High field matches the Vendor ID field in Router Configuration Space (4.1.1.3.3#9)
  - iii. Bytes 2 and 3 are 0 (4.1.1.3.3#6)
- b. For Register 1 (Product ID):
  - i. Verify that the Product ID Low field matches the Product ID field in Router Configuration Space (4.1.1.3.3#10)
  - ii. Verify that the Product ID High field matches the Product ID field in Router Configuration Space (4.1.1.3.3#11)
  - iii. Verify that bytes 2 and 3 are 0. (4.1.1.3.3#6)
- c. For register 7 (LRD Tuning) (Ver. 2 only):
  - i. Initiate RT Transaction from the Link Partner with Index 0 to Register 7 where bit 0 in byte 0 is set to 1b and bytes 1-3 and bits 1-7 in byte 0 are with random data.
  - ii. Verify that the Write to this register causes a write from the PUT with the same values written to this register except bit 0 in byte 0 which should be set to 0b
- d. For Register 8 (Opcode):
  - i. All bits are 0 (default value) (4.1.1.3.3#6)
- e. For Register 9 (Metadata):
  - i. All bits are 0 (default value) (4.1.1.3.3#6)
- f. For Register 12 (Link Configuration):
  - i. Bits 4 through 7 of byte 0 are 0 (reserved) (4.1.1.3.3#6)
  - ii. For a DFP, *Enabling Request* (Lane 1) is 0b if x1 Link (4.1.1.3.3#18)
  - iii. Bits 2 and 3 in byte 1 are 0 (reserved) (4.1.1.3.3#6)
  - iv. *Enabling Decision (Lane 0)* is 1b (4.1.2.3#4, 4.1.1.3.3#13)
  - v. *Enabling Decision (Lane 1)* is 1b if Link is x2 (4.1.2.3#4, 4.1.1.3.3#14)
  - vi. *Enabling Decision (Lane 1)* is 0b if Link is x1 (4.1.2.3#6)
  - vii. *Asymmetric Decision (Tx)* is 1b if PUT is 3 Tx
  - viii. *Asymmetric Decision (Tx)* is 0b if PUT is 3 Rx, Symmetric, x2, or x1.
  - ix. *Asymmetric Decision (Rx)* is 1b if PUT is 3 Rx
  - x. *Asymmetric Decision (Rx)* is 0b if PUT is 3 Tx, Symmetric, x2, or x1.
  - xi. For a DFP, *Gen 3 Support* bit is 1b if all of the following are true: (4.1.1.3.3#19)
    - a. On-Board Re-timers connected between the PUT and the cable support Gen 3 speeds (USB4\_Max\_Speed field in VIF is Gen 3 or higher)
    - b. The *Target Link Speed* field in the Lane Adapter Configuration Capability is 1100b (Gen 3) or 1110b (Gen 4)
  - xii. For a DFP, *Gen 3 Support* bit is 0b if any of the following are true: (4.1.1.3.3#20)
    - a. On-Board Re-timers connected between the PUT and the cable do not support Gen 3 speeds (USB4\_Max\_Speed field in VIF is Gen 2)
    - b. The *Target Link Speed* field in the Lane Adapter Configuration Capability is 1000b (Gen 2)
  - xiii. For a DFP operating at Gen 2 speed, *RS-FEC Request (Gen 2)* bit is the same as the *Request RS-FEC Gen 2* bit in the USB4 Port Capability of the PUT (4.1.1.3.3#21)
  - xiv. For a DFP operating at Gen 3 speed, *RS-FEC Request (Gen 3)* bit is the same as the *Request RS-FEC Gen 3* bit in the USB4 Port Capability of the PUT (4.1.1.3.3#22)

- xv. *USB4 Sideband Channel* field is 1b (4.1.1.3.3#23)
- xvi. *TBT3-Compatible Speeds Supported* bit is 0b if PUT does not support TBT3-compatible speeds (USB4\_TBT3\_Compatibility\_Supported field in VIF is NO) (4.1.1.3.3#24)
- xvii. Bits 2 through 7 in byte 2 are 0 (reserved) (4.1.1.3.3#6) (Ver. 1 only)
- g. For Register 12 (Link Configuration) (Ver. 2 only):
  - a. For a DFP, Gen 4 Support field is 1b if all the following are true:
    - i. The USB4 Port supports Gen 4 speed.
    - ii. All On-Board Re-timers connected between the USB4 Port and the cable support Gen 4 speed.
    - iii. The Target Link Speed field in the Lane 0 Adapter Configuration Capability is 1110b.
  - b. For a DFP, Gen 4 Support field is 0b if any of the following are true:
    - i. The USB4 Port does not support Gen 4 speed.
    - ii. On-Board Re-timers connected between the USB4 Port and the cable does not support Gen 4 speed.
    - iii. The Target Link Speed field in the Lane 0 Adapter Configuration Capability is 1100b or 1000b (Gen 2/3).
  - c. For DFP, Asymmetric Support 3 Tx field is 1b if all the following are true:
    - i. The USB4 Port supports Gen 4 speed and Asymmetric Link with three transmitters (bit 22 is 1b in the Asymmetric Support field).
    - ii. All On-Board Re-timers connected between the USB4 Port and the Cable support Gen 4 speed and Asymmetric Link with three transmitters.
  - d. For DFP, Asymmetric Support 3 Tx field is 0b if any of the following are true:
    - i. The USB4 Port does not support Gen 4 speed or Asymmetric Link with three transmitters (bit 22 is 0b in the Asymmetric Support field).
    - ii. On-Board Re-timers connected between the USB4 Port and the Cable do not support Gen 4 speed or Asymmetric Link with three transmitters.
  - e. For DFP, Asymmetric Support 3 Rx field is 1b if all the following are true:
    - i. The USB4 Port supports Gen 4 speed and Asymmetric Link with three receivers (bit 23 is 1b in the Asymmetric Support field).
    - ii. All On-Board Re-timers connected between the USB4 Port and the Cable support Gen 4 speed and Asymmetric Link with three receivers.
  - f. For DFP, Asymmetric Support 3 Rx field is 0b if any of the following are true:
    - i. The USB4 Port does not support Gen 4 speed or Asymmetric Link with three transmitters (bit 23 is 0b in the Asymmetric Support field).
    - ii. On-Board Re-timers connected between the USB4 Port and the Cable do not support Gen 4 speed or Asymmetric Link with three receivers.
  - g. For DFP, Request Asymmetric Tx field is 1b if Target Asymmetric Link is set to 01b, otherwise it is 0b.
  - h. For DFP, Request Asymmetric Rx field is 1b if Target Asymmetric Link is set to 10b, otherwise it is 0b.
  - i. Bit 7 in byte 2 is 0 (reserved) (4.1.1.3.3#6)
- h. For Register 13 (Gen 2/3 TxFFE):
  - i. *Clock Switch Done (Lane 0)* bit is 1 (4.1.1.3.3#26, 4.1.2.5#5, 4.1.2.5#9rt)
  - ii. Bits 4 and 5 in byte 2 are 0 (reserved) (4.1.1.3.3#6)
  - iii. Bits 4 and 5 in byte 3 are 0 (reserved) (4.1.1.3.3#6)

- iv. If x1 Link, the *Clock Switch Done (Lane 1)* bit is 0 (4.1.1.3.3#27, 4.1.2.5#5, 4.1.2.5#9rt)
  - v. If x2 Link, the *Clock Switch Done (Lane 1)* bit is 1 (4.1.1.3.3#27, 4.1.2.5#5, 4.1.2.5#9rt)
  - i. For Register 14 (Gen 4 TxFFE) (Gen 4 only):
    - i. Bit 6 in Gen 4 Partner Rx Status & TxFFE Request byte is 0 (reserved)
  - j. For Register 18:
    - i. All bits are 0 (default value) (4.1.1.3.3#6)
30. If test repetition is for a x1 or Gen 4 Link, skip Part 6 and go to Part 7

#### Part 6 – Bonding (Gen 2 and Gen 3 x2 Link Only)

- 31. Set the *Lane Bonding* bit to 1b in the Adapter Configuration Space of Lane 0
- 32. (if using an Analyzer) Parse the Trace from the Analyzer and verify that the PUT puts 001b in the *Lane Bonding Target* field of all TS1 and TS2 Ordered Sets (4.2.2.2#1)
- 33. Verify that the PUT sends a Hot Unplug Event Packet for the Lane 1 Adapter in the DFP (4.2.2.2#5)

#### Part 7 – Configuration Space Verification

- 34. Read the *Adapter State* field of the Lane 0 Adapter
- 35. Verify that the Lane 0 Adapter is in CL0 state (4.2.2.2#3, 4.2.1.4.1#1)
- 36. Read the *Adapter State* field of the Lane 1 Adapter:
  - a. If Link is x2 or Gen 4, verify that state is CL0 (4.2.1.4.1#1)
  - b. If Link is x1, verify that state is Disabled
- 37. Read the USB4 Adapter Configuration Capability of the Lane 0 Adapter and verify:
  - a. Current Link Speed field is set to Gen 4 if Link is Gen 4 speed
  - b. *Current Link Speed* field is set to Gen 3 if Link is Gen 3 speed (4.1.2.3#11)
  - c. *Current Link Speed* field is set to Gen 2 if Link is Gen 2 speed (4.1.2.3#11)
  - d. Negotiated Link Width field in Lane 0 Adapter is Asymmetric Link with 3 transmitters if Link is Asymmetric Link with 3 transmitters
  - e. Negotiated Link Width field in Lane 0 Adapter is Asymmetric Link with 3 receivers if Link is Asymmetric Link with 3 receivers
  - f. *Negotiated Link Width* field in Lane 0 Adapter is x2 if Link is x2 (4.2.2.2#4)
  - g. *Negotiated Link Width* field in Lane 0 Adapter is x1 if Link is x1 (8.2.2.3#21)
- 38. Read the USB4 Port Capability of the PUT and verify:
  - a. *Bonding Enabled* is 1b for a x2 Link (4.1.2.3#7)
  - b. *Bonding Enabled* is 0b for a x1 Link (4.1.2.3#8)
  - c. *TBT3-Compatible Mode* bit is set to 0b
  - d. If speed is Gen 2 and RS-FEC is on, *RS-FEC Enabled (Gen 2)* bit is 1b (4.1.2.3#14)
  - e. If speed is Gen 2 and RS-FEC is off, *RS-FEC Enabled (Gen 2)* bit is 0b (4.1.2.3#14)
  - f. If speed is Gen 3 and RS-FEC is on, *RS-FEC Enabled (Gen 3)* bit is 1b (4.1.2.3#17)
  - g. If speed is Gen 3 and RS-FEC is off, *RS-FEC Enabled (Gen 3)* bit is 0b (4.1.2.3#17)
- 39. Stop Analyzer (if using an Analyzer)

#### TD 4.006 DFP Lane Disable/Enable Test (DFP Only)

*Note: This test is only performed on the DFP. The test is performed simultaneously for both the Lane 0 Adapter and the Lane 1 Adapter of the Port being tested.*

- A. Purpose:
  - Verify that a DFP transitions into Disabled state correctly after being disabled
  - Verify that a DFP exits Disabled state correctly after being enabled
- B. Asserts:
  - 4.2.1.1.1#1, 4.2.1.1.1#2
  - 4.2.1.2.2#2
  - 4.2.1.3.3#5
  - 4.2.2.4#1
- C. Test Setups
  - AN\_HOST\_DFP1/ DC\_HOST\_DFP1 (Host)
  - AN\_HUB\_DFP1/ DC\_HUB\_DFP1 (Hub)
- D. Repetitions:
  - Repeat at Gen 2 and Gen 3 speeds (if supported)
- E. Background Check:
  - Gen 2/Gen 3 Lane 0/Lane 1 Background Check (if using an Analyzer)
- F. Procedure:

USB4 CV performs the following steps:

##### Part 0 – Setup

1. Start Analyzer
2. Reset UUT
3. Enumerate UUT Router
4. Set the following fields in the Adapter Configuration Space of both Lane Adapters:
  - a. *Link Credits Allocated* = 2
  - b. *Inter-Domain Time Initiator* = 1b
  - c. *Target Link Width* = 0000 11b
  - d. *Lane Bonding* = 1b
5. Reset the PUT:
  - a. Set the *Downstream Port Reset* bit to 1b
  - b. Wait for 10ms
  - c. Set the *Downstream Port Reset* bit to 0b
  - d. Wait for Lane Initialization to complete on both Lanes
6. In the PUT, set the *Lock* bit to 0b
7. Enumerate the KG Device Router

##### Part 1 – Lane 1 Adapter Disabled then Enabled

8. Set the *Lane Disable* bit in the Adapter Configuration Space of the Lane 1 Adapter to 1b
9. Reset the PUT:
  - a. Set the *Downstream Port Reset* bit to 1b
  - b. Wait for 10ms
  - c. Set the *Downstream Port Reset* bit to 0b
  - d. Wait for Lane Initialization to complete on Lane 0
10. In the PUT, set the *Lock* bit to 0b



11. Enumerate the KG Device Router
12. Read the Adapter State of Lane 1 and Lane 0
13. Verify that the Lane 1 Adapter is in the Disabled state (4.2.1.1.1#1)
14. Verify that the Lane 0 Adapter is in CL0 state (4.2.2.4#1)
15. Set the *Lane Disable* bit in the Adapter Configuration Space of the Lane 1 Adapter to 0b
16. Reset the PUT:
  - a. Set the *Downstream Port Reset* bit to 1b
  - b. Wait for 10ms
  - c. Set the *Downstream Port Reset* bit to 0b
  - d. Wait for Lane Initialization to complete on both Lanes
17. In the PUT, set the *Lock* bit to 0b
18. Enumerate the KG Device Router
19. Verify that the PUT sends a Hot Plug Event Packet with UPG = 0b for the Lane 1 Adapter (4.2.1.3.3#5)
20. Verify that the Lane 0 Adapter and the Lane 1 Adapter are both in the CL0 state

#### Part 2 – Both Lanes Disabled, then Enabled

21. Set the *Lane Disable* bit in the Adapter Configuration Space of the Lane 1 Adapter to 1b
22. Verify that the PUT sends a Hot Plug Event Packet with UPG = 1b for the Lane 1 Adapter (4.4.6.2.1#2)
23. Reset the PUT:
  - a. Set the *Downstream Port Reset* bit to 1b
  - b. Wait for 10ms
  - c. Set the *Downstream Port Reset* bit to 0b
  - d. Wait for Lane Initialization to complete on Lane 0
24. In the PUT, set the *Lock* bit to 0b
25. Enumerate the KG Device Router
26. Set the *Lane Disable* bit in the Adapter Configuration Space of the Lane 0 Adapter to 1b
27. Read the *Plugged* bit in the Adapter Configuration Space of the Lane 0 Adapter
28. Verify that the *Plugged* bit is 0b for the Lane 0 Adapter (4.2.1.1.1#2)
29. Read the Adapter State of Lane 1 and Lane 0
30. Verify that the Lane 1 Adapter is in the Disabled state (4.2.1.1.1#1, 4.4.6.2.1#3)
31. Verify that the Lane 0 Adapter is in the Disabled state (4.2.1.1.1#1, 4.4.6.2.1#3)
32. Set the *Lane Disable* bit in the Adapter Configuration Space of the Lane 0 Adapter to 0b
33. Reset the PUT:
  - a. Set the *Downstream Port Reset* bit to 1b
  - b. Wait for 10ms
  - c. Set the *Downstream Port Reset* bit to 0b
  - d. Wait for Lane Initialization to complete on Lane 0
34. In the PUT, set the *Lock* bit to 0b
35. Enumerate the KG Device Router
36. Verify that the PUT sends a Hot Plug Event Packet with UPG = 0b for the Lane 0 Adapter (4.2.1.3.3#5)
37. Verify that the Lane 0 Adapter is in the CL0 state
38. Set the *Lane Disable* bit in the Adapter Configuration Space of the Lane 1 Adapter to 0b
39. Reset the PUT:
  - a. Set the *Downstream Port Reset* bit to 1b
  - b. Wait for 10ms
  - c. Set the *Downstream Port Reset* bit to 0b
  - d. Wait for Lane Initialization to complete on both Lanes
40. In the PUT, set the *Lock* bit to 0b
41. Enumerate the KG Device Router

42. Verify that the PUT sends a Hot Plug Event Packet with UPG = 0b for the Lane 1 Adapter (4.2.1.3.3#5)
43. Verify that the Lane 0 Adapter and the Lane 1 Adapter are both in the CL0 state

#### Part 3 – Configuration Space Validation

44. Read the Adapter Configuration space of the Lane 1 Adapter and verify that the following fields have default values (4.4.6.2.1.1#2)
  - a. *Link Credits Allocated* = 0
  - b. *Inter-Domain Time Initiator* = 0b
  - c. *Target Link Width* = 000 01b
  - d. *Lane Bonding* = 0b
45. Read the Adapter Configuration space of the Lane 0 Adapter and verify that the following fields have default values (4.4.5.2.1#7)
  - a. *Link Credits Allocated* = 0
  - b. *Inter-Domain Time Initiator* = 0b
  - c. *Target Link Width* = 000 01b
  - d. *Lane Bonding* = 0b
46. Stop Analyzer

#### TD 4.007 UFP Lane Disable/Enable Test (UFP Only)

*Note: This test is only performed on the UFP. The test is performed simultaneously for both the Lane 0 Adapter and the Lane 1 Adapter of the Port being tested.*

- A. Purpose:
  - Verify that UFP Adapters transition into Disabled state correctly when Link Partner is disabled
  - Verify that UFP Adapters exit Disabled state correctly when Link Partner is enabled
- B. Asserts:
  - 4.2.1.2.2#2, 4.4.6.2.1.1#1-3
  - 4.4.6.2.1.2#1, 4.4.6.2.1.2#2, 4.4.6.2.1.2#4
- C. Test Setups
  - AN\_DEV\_UFP1 (Device)
  - AN\_HUB\_UFP1 (Hub)
- D. Repetitions:
  - Repeat at Gen 2 and Gen 3 speeds (if supported)
- E. Background Check:
  - Gen 2/Gen 3 Lane 0/Lane 1 Background Check
- F. Procedure:

USB4 CV does the following:

##### Part 0 – Setup

1. Start Analyzer
2. Reset UUT
3. Enumerate UUT Router
4. Initiate Lane Bonding

##### Part 1 – Lane 1 is Disabled, then Enabled

5. In the Link Partner of the PUT, set the *Lane Disable* bit in the Adapter Configuration Space of the Lane 1 Adapter to 1b
6. Reset the Link Partner of the PUT:
  - a. Set the *Downstream Port Reset* bit to 1b
  - b. Wait for 10ms
  - c. Set the *Downstream Port Reset* bit to 0b
  - d. Wait for Lane Initialization to complete on Lane 0
7. Wait 1 second
8. Verify that the PUT does not start Lane Initialization for Lane 1 (4.2.1.2.2#2)
9. Re-enumerate the Router
10. In the Link Partner of the PUT, set the *Lane Disable* bit in the Adapter Configuration Space of the Lane 1 Adapter to 0b
11. Reset the Link Partner of the PUT:
  - a. Set the *Downstream Port Reset* bit to 1b
  - b. Wait for 10ms
  - c. Set the *Downstream Port Reset* bit to 0b
12. Verify that the PUT starts Lane Initialization on Lane 1 (4.2.1.2.2#2)
13. Wait for Lane Initialization to complete

14. In the PUT, set the *Lock* bit to 0b
15. Enumerate the KG Device Router

Part 2 – Both Lanes are Disabled, then Enabled

16. In the Link Partner of the PUT, set the *Lane Disable* bit in the Adapter Configuration Space of the Lane 1 Adapter to 1b
17. In the Link Partner of the PUT, set the *Lane Disable* bit in the Adapter Configuration Space of the Lane 0 Adapter to 1b
18. Reset the Link Partner of the PUT:
  - a. Set the *Downstream Port Reset* bit to 1b
  - b. Wait for 10ms
  - c. Set the *Downstream Port Reset* bit to 0b
19. Verify that the PUT Drives SBTX to logical low for tDisconnectTx (4.4.6.2.1.2#1)
20. In the Link Partner of the PUT, set the *Lane Disable* bit in the Adapter Configuration Space of the Lane 1 Adapter to 0b
21. In the Link Partner of the PUT, set the *Lane Disable* bit in the Adapter Configuration Space of the Lane 0 Adapter to 0b
22. Reset the Link Partner of the PUT:
  - a. Set the *Downstream Port Reset* bit to 1b
  - b. Wait for 10ms
  - c. Set the *Downstream Port Reset* bit to 0b
23. Verify that the PUT starts Lane Initialization from Phase 1 (4.4.6.2.1.2#4)
24. Wait for Lane Initialization to finish

TD 4.008    Deprecated

## TD 4.009 Lane Initialization Adapter State Test

*Note: The test is performed simultaneously for both the Lane 0 Adapter and the Lane 1 Adapter of the Port being tested.*

### A. Purpose:

- Verify that the PUT transitions between states correctly during Lane Initialization

### B. Asserts:

- 4.2.1.2.3#2
- 4.2.1.3.2#1
- 4.2.1.3.3#1, 4.2.1.3.3#6
- 4.2.1.3.4#5-6
- 4.2.1.3.5#3-5 4.2.1.3.5#8 4.2.1.3.5#11
- 4.2.1.4.1#1
- 4.2.1.4.3#8, 4.2.1.4.3#9
- 4.2.1.5.1#1, 4.2.1.5.1#2
- 4.2.1.5.2#1
- 4.2.1.5.3#1
- 4.2.1.5.3#3 4.2.1.5.3#2
- 4.2.1.4.1#2
- 4.2.2.2#2
- 4.2.2.2.1#3
- 4.4.4#3-8

### C. Test Setups

- AN\_HOST\_DFP1 (Host)
- AN\_DEV\_UFP1 (Device)
- AN\_HUB\_UFP1 (Hub UFP)
- AN\_HUB\_DFP1 (Hub DFP)

### D. Repetitions:

- Repeat at Gen 2 and Gen 3 speeds (if supported)
- Repeat with bonding initiated as follows:
  - Send TS1 OS to PUT
  - Set Lane Bonding bit to 1b in the Lane 0 Adapter
  - Set Lane Bonding bit to 1b in the Lane 1 Adapter

### E. Background Check:

- Gen 2/Gen 3 Lane 0/Lane 1 Background Check

### F. Procedure:

USB4 CV performs the following steps:

#### Part 0 – Setup

1. Start Analyzer
2. Reset PUT
3. Start Lane Initialization

## Part 1 – Training State

4. If there are no re-timers on the Link;
  - a. Verify that:
    - i. PUT starts sending back-to-back SLOS1, which indicates entry to Training.LOCK1 sub-state (4.2.1.2.3#2)
  - b. Verify that the PUT sends back-to-back SLOS1 until all of the following are true: (4.2.1.3.2#1)
    - i. KG Host/Device sent at least 2 SLOS1 symbols to PUT
    - ii. PUT sent at least 2 complete SLOS1
5. Verify that:
  - a. PUT starts sending back-to-back SLOS2, which indicates entry to Training.LOCK2 sub-state (4.2.1.3.2#1)
  - b. If operating at Gen 2 speed (RS-FEC disabled), PUT sends 32 SLOS2 symbols for each SLOS2 (4.2.1.3.4#5, 4.2.1.3.4#7)
  - c. Else, PUT sends 16 SLOS2 symbols for each SLOS2 (4.2.1.3.4#6, 4.2.1.3.4#7)
6. Verify that the PUT sends back-to-back SLOS2 until all of the following are true: (4.2.1.3.2#1)
  - a. KG Host/Device sent at least 2 SLOS2 symbols
  - b. PUT sent at least 2 complete SLOS2
7. Verify that the PUT starts sending back-to-back TS1, which indicates entry to Training.TS1 sub-state (4.2.1.3.2#1)
8. Parse each TS1 Ordered set and verify that:
  - a. Bits 58:56 (*Lane Bonding Target*) are 000b if the *Target Link Width* field in the USB4 Adapter Configuration Capability is 000 01b (two Single-Lane Links) (4.2.1.3.5#3)
  - b. Bits 55:48 (*Lane Number*) are 00h if Ordered Set is on the Lane 0 (4.2.1.3.5#4)
  - c. Bits 55:48 (*Lane Number*) are 01h if Ordered Set is on the Lane 1 (4.2.1.3.5#4)
  - d. Bits 31:29 (*Reserved*) are 000b (4.2.1.3.5#5)
  - e. Bits 28:26 (*Lane Bonding Target 2*) match the *Lane Bonding Target* field (4.2.1.3.5#8)
  - f. Bits 9:0 (*SCR*) are 00 1111 0010b (4.2.1.3.5#11)
9. Verify that the PUT sends back-to-back TS1 until all of the following are true: (4.2.1.3.2#1)
  - a. KG Host/Device sent at least 2 TS1
  - b. If Gen 2, PUT sent at least 32 TS1
  - c. If Gen 3, PUT sent at least 16 TS1
10. Verify that the PUT transitions starts sending back-to-back TS2, which indicates entry to Training.TS2 sub-state (4.2.1.3.2#1)
11. Parse each TS2 Ordered set and verify that:
  - a. Bits 58:56 (*Lane Bonding Target*) are 000b if the *Target Link Width* field in USB4 Adapter Configuration Capability is 0000 01b (two Single-Lane Links) (4.2.1.3.5#3)
  - b. Bits 55:48 (*Lane Number*) are 00h if Ordered Set is on the Lane 0 (4.2.1.3.5#4)
  - c. Bits 55:48 (*Lane Number*) are 01h if Ordered Set is on the Lane 1 (4.2.1.3.5#4)
  - d. Bits 31:29 (*Reserved*) are 000b (4.2.1.3.5#5)
  - e. Bits 28:26 (*Lane Bonding Target 2*) match the *Lane Bonding Target* field (4.2.1.3.5#8)
  - f. Bits 9:0 (*SCR*) are 00 1111 0010b (4.2.1.3.5#11)
12. Verify that the PUT sends back-to-back TS2 until all of the following are true: (4.2.1.3.2#1)
  - a. KG Host/Device sent at least 2 TS2
  - b. If Gen 2, PUT sent at least 16 TS2
  - c. If Gen 3, PUT sent at least 8 TS2
13. Verify that the PUT transitions to CL0 state (i.e. stops sending TS2) within tTrainingAbort2 after it send the first SLOS1 symbol (4.2.1.3.3#1, 4.2.1.4.1#1)

## Part 2 – Bonding State

14. Initiate bonding (see repetitions)
15. Verify that the PUT starts sending back-to-back TS1 (which indicates entry to Bonding.TS1 state) after receiving 3 TS1 (4.2.1.4.3#8, 4.2.1.4.3#9, 4.2.1.5.1#1, 4.2.1.5.1#2)
16. Parse each TS1 Ordered set and verify that:
  - a. Bits 58:56 (*Lane Bonding Target*) are 001b if the *Target Link Width* field in the USB4 Adapter Configuration Capability is 0000 11b (Dual-Lane Link) (4.2.1.3.5#3)
  - b. Bits 55:48 (*Lane Number*) are 00h if Ordered Set is on the Lane 0 (4.2.1.3.5#4)
  - c. Bits 55:48 (*Lane Number*) are 01h if Ordered Set is on the Lane 1 (4.2.1.3.5#4)
  - d. Bits 31:29 (*Reserved*) are 000b (4.2.1.3.5#5)
  - e. Bits 28:26 (*Lane Bonding Target 2*) match the *Lane Bonding Target* field (4.2.1.3.5#8)
  - f. Bits 9:0 (*SCR*) are 00 1111 0010b (4.2.1.3.5#11)
17. Send back-to-back TS1 to the PUT
18. Verify that the PUT starts sending back-to-back TS2 (which indicates entry to Bonding.TS2 state) after all of the following are true: (4.2.1.5.2#1)
  - a. KG Host/Device sent at least 2 TS1
  - b. If Gen 2, PUT sent at least 32 TS1
  - c. If Gen 3, PUT sent at least 16 TS1
19. Parse each TS2 Ordered set and verify that:
  - a. Bits 58:56 (*Lane Bonding Target*) are 001b if the *Target Link Width* field in USB4 Adapter Configuration Capability is 0000 11b (Dual-Lane Link) (4.2.1.3.5#3)
  - b. Bits 55:48 (*Lane Number*) are 00h if Ordered Set is on the Lane 0 (4.2.1.3.5#4)
  - c. Bits 55:48 (*Lane Number*) are 01h if Ordered Set is on the Lane 1 (4.2.1.3.5#4)
  - d. Bits 31:29 (*Reserved*) are 000b (4.2.1.3.5#5)
  - e. Bits 28:26 (*Lane Bonding Target 2*) match the *Lane Bonding Target* field (4.2.1.3.5#8)
  - f. Bits 9:0 (*SCR*) are 00 1111 0010b (4.2.1.3.5#11)
20. Send back-to-back TS2 to the PUT
21. Verify that the PUT doesn't stop sending back-to-back TS2 until all of the following are true: (4.2.1.5.2#1, 4.2.1.5.3#1)
  - a. KG Host/Device sent at least 2 TS2
  - b. If Gen 2, PUT sent at least 16 TS2
  - c. If Gen 3, PUT sent at least 8 TS2
22. Verify that first PUT to transition to CL0 state sends TS2 until other PUT transitions to CL0 state (4.2.2.2.1#3, 4.2.1.5.3#3)
23. Verify that the PUT is in CL0 state (4.2.1.5.3#2, 4.2.1.4.1#2)
  - a. Verify that the PUT transitioned back to CL0 state within 40  $\mu$ s (min tBonding time) after sending the first TS1 Ordered Set with *Lane Bonding Target* set to 001b (4.2.2.2#2)
  - b. Verify that both Lanes transitioned from the Training state to the CL0 state within tTrainingAbort2 time. (4.2.2.2.1#2)

## Part 3 – CL0 State

24. Verify that:
  - a. PUT sends a de-skew Ordered Set on each lane after Adapter transitions to CL0 state (4.4.4#3)
  - b. De-Skew Ordered Set is only sent in direction exiting electrical idle (4.4.4#4)
  - c. De-skew OS are sent simultaneously (within permitted skew) (4.4.4#6)
  - d. Each de-skew Ordered Set is sent on both Lanes in the same locations within the Symbol (4.4.4#6)



- e. PUT sends a de-skew Ordered Set immediately after sending the last TS2 ordered set (4.4.4#8)
- 25. After transitioning to CL0 state, verify that the PUT sends only TS2 Ordered Sets before it sends a de-skew ordered set (4.4.4#9)
- 26. Read the *Plugged* bit and verify that it is 1b (4.2.1.3.3#6)
- 27. Stop Analyzer

TD 4.010	Moved to Exerciser Test
TD 4.011	Moved to Exerciser Test
TD 4.012	Moved to Exerciser Test
TD 4.013	Moved to Exerciser Tests
TD 4.014	Moved to Exerciser Tests
TD 4.015	Moved to Exerciser Tests
TD 4.016	Moved to Exerciser Tests

#### TD 4.017 UFP SBRX Disconnect Test (UFP Only)

*Note: This test is only performed on the UFP.*

- A. Purpose:
  - Verify that the PUT handles SBRX-initiated Disconnect on UFP correctly
- B. Asserts:
  - 4.4.5.1.1#1-4
- C. Repeat with the following Disconnect Events:
  - Router Hot Unplug (4.4.5.1.1#3) – disable/enable to generate
  - DFP Reset (4.4.5.1.1#4)
- D. Test Setups
  - AN\_DEV\_UFP1 (Device)
  - AN\_HUB\_UFP1 (Hub)
- E. Repetitions:
  - Repeat at Gen 2 and Gen 3 speeds (if supported)
- F. Background Check:
  - Gen 2/Gen 3 Lane 0/Lane 1 Background Check
- G. Procedure:

USB4 CV performs the following steps:

1. Start Analyzer
2. Reset UUT
3. Perform Lane Initialization
4. Initiate Lane Bonding
5. Wait for PUT Adapters to reach CL0 state
6. Set the following fields:
  - a. *Link Credits Allocated* = 2
  - b. *Inter-Domain Time Initiator* = 1b
  - c. *CL0s Enable* = 1b
  - d. *CL1 Enable* = 1b
  - e. *CL2 Enable* = 1b
7. Initiate Disconnect Event (see repetitions)
8. Verify that the PUT drives SBTX low for tDisconnectTx (4.4.5.1.1#1)

*Note: It is not a test failure if the PUT drives SBTX low one or more times before driving SBTX low for tDisconnectTx time.*

9. Read the following fields and verify default values: (4.4.5.1.1#2)
  - a. *Link Credits Allocated* = 0
  - b. *Inter-Domain Time Initiator* = 0b
  - c. *CL0s Enable* = 0b
  - d. *CL1 Enable* = 0b
  - e. *CL2 Enable* = 0b
  - f. *Lane Bonding* = 0b
10. Stop Analyzer

## TD 4.018 DFP SBRX Disconnect Test (DFP Only)

*Note: This test is only performed on the DFP.*

- A. Purpose:
  - Verify that the PUT handles SBRX-initiated Disconnect on the DFP correctly
- B. Asserts:
  - 4.4.5.2.1#1-3, 4.4.5.2.1#6, 4.4.5.2.1#7
- C. Test Setups
  - AN\_HOST\_DFP1 (Host)
  - AN\_HUB\_DFP1 (Hub)
- D. Repetitions:
  - Repeat at Gen 2 and Gen 3 speeds (if supported)
- E. Background Check:
  - Gen 2/Gen 3 Lane 0/Lane 1 Background Check
- F. Procedure:

USB4 CV performs the following steps:

1. Start Analyzer
2. Reset UUT
3. Enumerate UUT Router
4. Initiate Lane Bonding
5. Set the following fields:
  - a. *Link Credits Allocated* = 2
  - b. *Inter-Domain Time Initiator* = 1b
  - c. *CL0s Enable* = 1b
  - d. *CL1 Enable* = 1b
  - e. *CL2 Enable* = 1b
  - f. *Lane Disable* = 0b
6. Configure a Loopback Path
7. Send 16 packets on the Loopback Path
8. Wait for all 16 packets to be received back at the Host on the Loopback Path
9. Initiate a disconnect so that the Link Partner drives SBTX to logical low for tDisconnectRx
10. Verify that the PUT sends an LT\_LRoff Transaction (4.4.5.2.1#1)
11. Send 16 packets on the Loopback Path
12. Verify that the PUT does not forward any of the packets on the Loopback Path (i.e. none of the packets are received back at the Host) (4.4.5.2.1#2)
13. Verify that both PUT Adapters are in CLd state (4.4.5.2.1#3)
14. Verify that the PUT sends a Hot Unplug Event Packet with UPG = 1b for each enabled Adapter (4.4.5.2.1#6)
15. Read the following fields from the Adapter Configuration space of each PUT and verify that the following fields have default values (4.4.5.2.1#7):
  - a. *Link Credits Allocated* = 0
  - b. *Inter-Domain Time Initiator* = 0b
  - c. *CL0s Enable* = 0b
  - d. *CL1 Enable* = 0b
  - e. *CL2 Enable* = 0b
  - f. *Lane Bonding* = 0b

- g. *EnableUniDirectionalMode* = 0b
  - h. *Target Link Width* = 00001b
16. Stop Analyzer

TD 4.019    [Deprecated](#)

TD 4.020    [Tx Skew Test](#)

*Note : This test is not run if Time Synchronization Protocol Not Supported (TSNS) is 1.*

A. Purpose:

- Verify that the PUT transmitter does not exceed the maximum allowed skew

B. Asserts:

- 4.2.2.2#7

C. Test Setups

- AN\_HOST\_DFP1 (Host)
- AN\_DEV\_UFP1 (Device)
- AN\_HUB\_UFP1 (Hub UFP)
- AN\_HUB\_DFP1 (Hub DFP)

D. Repetitions:

- Repeat at the following Link configurations:
  - Gen 2 x2
  - Gen 3 x2 (if supported)
  - Gen 4 x2 (if supported)
  - Gen 4 Asymmetric 3 transmitters (if supported)
- Repeat test 10 times

E. Background Check:

- Gen 2/Gen 3 Lane 0/Lane 1 Background Check

F. Procedure:

USB4 CV performs the following steps:

1. Start Analyzer
2. Reset UUT
3. Enumerate RUT
- ~~3.4.~~ If Gen 2 or Gen 3 link:
  - ~~a.~~ Enable bi-directional Time Sync Handshakes:
    - ~~i.~~ *TSPacketInterval* = 16 (HiFi)
    - ~~ii.~~ *EnableUniDirectionalMode* = 0
    - ~~iii.~~ *Disable Time Sync* = 0
5. If Gen 4 link:
  - a. Enable Enhanced Uni-directional Time Sync Handshakes:
    - i. *AdapterTimeSyncInterval* = 16 (HiFi)
    - ii. *Enable Enhanced Uni-Directional Mode* = 1
    - ~~iii.~~ *Disable Time Sync* = 0
- ~~5.6.~~ Wait 5 milliseconds
- ~~6.7.~~ Stop Analyzer
- ~~7.8.~~ Parse analyzer trace and verify that skew between all enabled transmitters does not exceed LANE\_TO\_LANE\_SKEW (26ns)

TD 4.021    [Deprecated](#)

TD 4.022    ~~Deprecated~~



TD 4.023    **Deprecated**

TD 4.024    **Deprecated**

TD 4.025    Deprecated

TD 4.101            **Gen 4 Lane Initialization Adapter State Test**

*Note: This test only applies to a PUT that supports Gen 4 speed.*

- A. Purpose:
  - Verify that the PUT transitions between states correctly during Lane Initialization
- B. Asserts:
  - 4.2.1.6.5#1, 4.2.1.6.5.1#1-4, 4.2.1.6.5.1#8-9, 4.2.1.6.5.2#1, 4.2.1.6.5.2#4-6, 4.2.1.6.5.3#1-5
- C. Test Setups
  - AN\_HOST\_DFP1 (Host)
  - AN\_DEV\_UFP1 (Device)
  - AN\_HUB\_UFP1 (Hub UFP)
  - AN\_HUB\_DFP1 (Hub DFP)
- D. Repetitions:
  - None
- E. Procedure:

USB4 CV performs the following steps:

Part 0 - Setup

1. Start Analyzer
2. Reset PUT
3. Start Lane Initialization

Part 1 – Training State

4. Verify that PUT starts sending back-to-back Gen 4 TS1, which indicates entry to Training.TS1 sub-state
5. Verify that the PUT sends back-to-back Gen 4 TS1 until all of the following are true:
  - a. KG Host/Device sent Gen 4 TS1 with Indication field set to 2h or Gen 4 TS2 to all enabled transmitters in PUT
  - b. PUT sent at least 16 consecutive Gen 4 TS1 with Indication field set to 2h on all enabled transmitters.
6. Verify that PUT starts sending back-to-back Gen 4 TS2 which indicates entry to Training.TS2 sub-state
7. Transition to Training.TS2 sub-state occurs within tGen4TS1 time (i.e. there is no more than tGen4TS1 time between the PUT sending the first Gen 4 TS1 and sending the first bit of the first Gen 4 TS2)
8. Verify that the PUT sends back-to-back Gen 4 TS2 until all of the following are true:
  - a. KG Host/Device sent Gen 4 TS2 with Indication field set to 4h or Gen 4 TS3 on all enabled transmitters.
  - b. PUT sent at least 16 consecutive Gen 4 TS2 with Indication field set to 4h on all enabled transmitters
9. If there are On-board Re-timer on the DUT assembly, verify that the PUT sends TS2.clksw for tPreClkSw+tClkSwPeriod time.
10. Verify that the PUT starts sending back-to-back TS3, which indicates entry to Training.TS3 sub-state

11. Transition to Training.TS3 sub-state occurs within tGen4TS2 time (i.e. there is no more than tGen4TS2 time between the PUT sending the first trit of the first TS2 and sending the first trit of the first TS3)
12. Verify that the PUT sends back-to-back TS3 until all of the following are true:
  - a. KG Host/Device sent Gen 4 TS3 with Indication field set to 6h on all enabled transmitters.
  - b. PUT sent at least 16 Gen 4 TS3 with Indication field set to 6h.
13. Verify that the PUT transitions starts sending back-to-back Gen 4 TS4, which indicates entry to Training.TS4 sub-state
14. Verify that the PUT sends back-to-back Gen 4 TS4 with Counter field set to 0h and then increases the Counter field from 1h to Fh.
15. Verify that the same Gen 4 TS4 is sent on all enabled transmitters.
16. Verify that the PUT transitions to CL0 state (i.e. stops sending Gen 4 TS4) after sending the Gen 4 TS4 with Counter field set to Fh

#### Part 2 – CL0 State

17. Verify that:
  - a. PUT sends a De-Skew Block on all the enabled transmitters that transition to CL0 state
  - b. De-Skew Block is sent simultaneously (within permitted skew)
  - c. PUT sends a De-Skew Block immediately after sending the last Gen 4 TS4
18. Read the Plugged bit and verify that it is 1b
19. Stop Analyzer

*Note: This test only applies to a PUT that supports Gen 4 speed.*

- A. Purpose:
  - Verify that the PUT enters CL2 state correctly when there are no Re-timers on the Link
  - Verify that the PUT exits CL2 state correctly when there are no Re-timers on the Link
- B. Asserts:
  -
- C. Test Setups
  - AN\_HOST\_DFP1 (Host)
  - AN\_DEV\_UFP1 (Device)
  - AN\_HUB\_UFP1 (Hub UFP)
  - AN\_HUB\_DFP1 (Hub DFP)
- D. Repetitions:
  - Repeat with:
    - PUT initiating CL2 first
    - PUT initiating CL2 after already in CL0s
    - Re-timers on Link
  - Repeat with:
    - EXIT\_TIME =
    - EXIT\_TIME = 5 minutes
    - Symmetric
    - Asymmetric 3 transmitter
    - Asymmetric 3 receivers
- E. Procedure:

USB4 CV performs the following steps:

Part 0 - Setup

1. Reset UUT
2. Enumerate UUT Router
3. Read the CL2 Support bit in the PUT
4. Do not enable Time Sync Handshakes
5. Enable CLx states in the PUT:
  - a. CL2 Enable = 1b (if PUT initiating CL2 first) or 0b (if PUT initiating CL2 after already in CL0s)
  - b. CL1 Enable = 0b
  - c. CL0s Enable = 1b
6. Enable CLx states in the Link Partner:
  - a. CL2 Enable = 0b (if PUT initiating CL2 first) or 1b (if PUT initiating CL2 after already in CL0s)
  - b. CL1 Enable = 0b
  - c. CL0s Enable = 1b
7. If CL2 Enable in the PUT is set to 0b continue to Part 2, else continue to Part 1

Part 1 – PUT Sends CL\_OFF while in CL0

8. Verify that the PUT sends at least 24 CL\_OFF Ordered Sets with index field set to 0 and CLx state field set to 2t.
9. Verify that the PUT sends 102 CL\_OFF Ordered Sets or valid Data Sets
10. If there are Re-timers on the Link repeat the following steps for each Re-timer i=1..number of Re-timers:

- a. Verify that the PUT sends at least 24 CL\_OFF Ordered Sets with index field set to i and CLx state field set to 2t.
  - b. Verify that the PUT sends 102 CL\_OFF Ordered Sets or valid Data Sets
- 11. Verify that the PUT is in CL0s (Tx) state
- 12. Verify that transmitter is in electrical idle
- 13. Verify that Lane common mode voltages are maintained
- 14. Continue to Part 2

#### Part 2 – Link Partner Sends CL\_OFF

- 15. If not enabled, enable CLx states in the Link Partner:
  - a. CL2 Enable = 1b
- 16. Link Partner sends 24 CL\_OFF Ordered Sets with Index field set to 0t and CLx state set to 2t, followed by 102 valid Data Sets. No Redundancy Sets are sent
- 17. If there are Re-timers on the Link, the Link partner send the following for each Re-timer i=1..number of Re-timers:
  - a. Link Partner sends at least 24 CL\_OFF Ordered Sets with index field set to i and CLx state field set to 2t.
  - b. Link Partner sends 102 CL\_OFF Ordered Sets or valid Data Sets
- 18. Verify that the PUT enters CL2 state (if Part 1 was executed) or CL0s (Rx) (If Part 1 wasn't executed)
- 19. Verify that receiver termination is maintained
- 20. If PUT in CL2, continue to Part 4, else continue to Part 3

#### Part 3 – PUT Sends CL\_OFF while in CL0s (Rx)

- 21. If not enabled, enable CLx states in the PUT:
  - a. CL2 Enable = 1b
- 22. Verify that the PUT sends at least 24 CL\_OFF Ordered Sets with index field set to 0 and CLx state field set to 2t.
- 23. Verify that the PUT sends 102 CL\_OFF Ordered Sets or valid Data Sets
- 24. If there are Re-timers on the Link repeat the following steps for each Re-timer i=1..number of Re-timers:
  - a. Verify that the PUT sends at least 24 CL\_OFF Ordered Sets with index field set to i and CLx state field set to 2t.
  - b. Verify that the PUT sends 102 CL\_OFF Ordered Sets or valid Data Sets
- 25. Verify that the PUT is in CL2 state
- 26. Verify that transmitter is in electrical idle
- 27. Verify that Lane common mode voltages are maintained

#### Part 4 – CL2 Exit

- 28. Wait EXIT\_TIME time after detecting that the PUT transitioned to CL2 state (see repetitions)
- 29. Send the PUT a Read Request to cause the PUT Adapters to exit the CL2 state
- 30. If the Link Partner initiated CL2 exit, verify that the PUT does the following:
  - a. Sends an LFPS burst on Lane 0 for at least 16 LFPS cycles
  - b. Stop sending LFPS tStopLFPS2 after sending at least 16 LFPS cycles and LFPS ended on its receiver
  - c. Sends the first LFPS within tWarmUpCL2 after receiving the first LFPS cycle
  - d. Returns to Electrical Idle for tPreData
  - e. Starts transmitting Gen 4 TS1 on all the enabled Lanes

- f. Enables the receiver to start bit and symbol synchronization not earlier than  $t_{CLxIdleRx}$  after the last LFPS cycle received
  - g. Completes Symbol lock within  $t_{RxLock}$  time
- 31. If the PUT initiated CL2 exit, verify that the PUT does the following:
  - a. Send a Low Frequency Periodic Signaling (LFPS) burst on Lane 0 until the receiver detects LFPS and the transmitter sent at least 16 LFPS cycles after the receiver detected the LFPS
  - b. Return to Electrical Idle for  $t_{PreData}$
  - c. Start transmitting Gen 4 TS1 on all the enabled Lanes
  - d. PUT Adapters complete Symbol lock within  $t_{RxLock}$  time
  - e. PUT Adapters transition to Training.TS1 sub-state
- 32. Verify that the PUT transitions to CL0 state



*Note: This test only applies to a PUT that supports Gen 4 speed.*

- A. Purpose:
  - Verify that the PUT enters CL1 state correctly when there are no Re-timers on the Link
  - Verify that the PUT exits CL1 state correctly when there are no Re-timers on the Link
- B. Asserts:
  -
- C. Test Setups
  - AN\_HOST\_DFP1 (Host)
  - AN\_DEV\_UFP1 (Device)
  - AN\_HUB\_UFP1 (Hub UFP)
  - AN\_HUB\_DFP1 (Hub DFP)
- D. Repetitions:
  - Repeat with:
    - PUT initiating CL1 first
    - PUT initiating CL1 after already in CL0s
    - Re-timers on Link
  - Repeat with:
    - EXIT\_TIME =
    - EXIT\_TIME = 5 minutes
    - Symmetric
    - Asymmetric 3 transmitter
    - Asymmetric 3 receivers
- E. Procedure:

USB4 CV performs the following steps:

#### Part 0 – Setup

1. Reset UUT
2. Enumerate UUT Router
3. Read the CL1 Support bit in the PUT
4. Do not enable Time Sync Handshakes
5. Enable CLx states in the PUT and in the Link Partner:
  - a. CL1 Enable = 1b (if PUT initiating CL1 first) or 0b (if PUT initiating CL1 after already in CL0s)
  - b. CL2 Enable = 0b
  - c. CL0s Enable = 1b
6. If CL1 Enable is set to 0b continue to Part 2, else continue to Part 1

#### Part 1 – PUT Sends CL\_OFF while in CL0

7. Verify that the PUT sends at least 24 CL\_OFF Ordered Sets with index field set to 0 and CLx state field set to 1t.
8. Verify that the PUT sends 102 CL\_OFF Ordered Sets or valid Data Sets
9. If there are Re-timers on the Link repeat the following steps for each Re-timer i=1..number of Re-timers:
  - a. Verify that the PUT sends at least 24 CL\_OFF Ordered Sets with index field set to i and CLx state field set to 1t.

- b. Verify that the PUT sends 102 CL\_OFF Ordered Sets or valid Data Sets
- 10. Verify that the PUT is in CL0s (Tx) state
- 11. Verify that transmitter is in electrical idle
- 12. Verify that Lane common mode voltages are maintained
- 13. Continue to Part 2

#### Part 2 – Link Partner Sends CL\_OFF

- 14. Link Partner sends 24 CL\_OFF Ordered Sets with Index field set to 0t and CLx state set to 1t, followed by 102 valid Data Sets. No Redundancy Sets are sent
- 15. If there are Re-timers on the Link, the Link partner send the following for each Re-timer i=1..number of Re-timers:
  - a. Link Partner sends at least 24 CL\_OFF Ordered Sets with index field set to i and CLx state field set to 1t.
  - b. Link Partner sends 102 CL\_OFF Ordered Sets or valid Data Sets
- 16. Verify that the PUT enters CL1 state (if Part 1 was executed) or CL0s (Rx) (If Part 1 wasn't executed)
- 17. If PUT in CL1, continue to Part 4, else continue to Part 3

#### Part 3 – PUT Sends CL\_OFF while in CL0s (Rx)

- 18. Verify that the PUT sends at least 24 CL\_OFF Ordered Sets with index field set to 0 and CLx state field set to 1t.
- 19. Verify that the PUT sends 102 CL\_OFF Ordered Sets or valid Data Sets
- 20. If there are Re-timers on the Link repeat the following steps for each Re-timer i=1..number of Re-timers:
  - a. Verify that the PUT sends at least 24 CL\_OFF Ordered Sets with index field set to i and CLx state field set to 1t.
  - b. Verify that the PUT sends 102 CL\_OFF Ordered Sets or valid Data Sets
- 21. Verify that the PUT is in CL1 state
- 22. Verify that transmitter is in electrical idle
- 23. Verify that Lane common mode voltages are maintained

#### Part 4 – CL1 Exit

- 24. Wait EXIT\_TIME time after detecting that the PUT transitioned to CL1 state (see repetitions)
- 25. Send the PUT a Read Request to cause the PUT Adapters to exit the CL1 state
- 26. If the Link Partner initiated CL1 exit, verify that the PUT does the following:
  - a. Sends an LFPS burst on Lane 0 for at least 16 LFPS cycles
  - b. Stop sending LFPS tStopLFPS2 after sending at least 16 LFPS cycles and LFPS ended on its receiver
  - c. Sends the first LFPS within tWarmUpCL1 after receiving the first LFPS cycle
  - d. Returns to Electrical Idle for tPreData from last LFPS to transmitting Gen 4 TS1
  - e. Starts transmitting Gen 4 TS1 on all the enabled Lanes
  - f. Completes Symbol lock within tCLxIdleRx+tRxLock time after the last LFPS cycle received
- 27. If the PUT initiated CL1 exit, verify that the PUT does the following:
  - a. Send a Low Frequency Periodic Signaling (LFPS) burst on Lane 0 until the receiver detects LFPS and the transmitter sent at least 16 LFPS cycles after the receiver detected the LFPS
  - b. Return to Electrical Idle for tPreData from last LFPS to transmitting Gen 4 TS1
  - c. Start transmitting Gen 4 TS1 on all the enabled Lanes
  - d. PUT Adapters complete Symbol lock within tRxLock time

- e. PUT Adapters transition to Training.TS1 sub-state
28. Verify that the PUT transitions to CL0 state withing tTrainingAbort2 time

## TD 4.104      Gen 4 CL0s Test

*Note: This test only applies to a PUT that supports Gen 4 speed.*

*Note: This test is not performed if the Router does not support CL0s state.*

- A. Purpose:
  - Verify that the PUT Adapters enter CL0s state correctly
  - Verify that the PUT Adapters exit CL0s state correctly
- B. Asserts:
  -
- C. Test Setups
  - AN\_HOST\_DFP1 (Host)
  - AN\_DEV\_UFP1 (Device)
  - AN\_HUB\_UFP1 (Hub UFP)
  - AN\_HUB\_DFP1 (Hub DFP)
- D. Repetitions:
  - Repeat with:
    - EXIT\_TIME =
    - EXIT\_TIME = 5 minutes
    - Without Re-timers
    - With Re-timers
    - CL0s Rx
    - CL0s Tx
    - Symmetric
    - Asymmetric 3 transmitter
    - Asymmetric 3 receivers
- E. Procedure

USB4 CV performs the following steps:

### Part 0 - Setup

1. Reset UUT
2. Enumerate UUT Router
3. Read the CL0s Support bit in PUT
4. Enable CLx states in the PUT:
  - a. CL2 Enable = 0b
  - b. CL1 Enable = 0b
  - c. CL0s Enable = 1b
5. Enable CLx states in the Link Partner:
  - a. CL2 Enable = 0b
  - b. CL1 Enable = 1b
  - c. CL0s Enable = 1b

### Part 1 – Initiate CL0s Entry by Link Partner:

6. Wait for the Link Partner to send Gen 4 CL\_OFF Ordered Sets
7. Verify that the PUT transitions to CL0s (Rx) state after receiving CL\_OFF Ordered Sets
8. Verify that the PUT transmitter is still sending valid data

## Part 2 –Initiate CL0s Exit by Link Partner

9. Send a Read Request to cause the Link Partner Adapters to exit the CL0s state
10. Link Partner will transmit LFPS
11. Verify that the PUT sends 24 CL0s\_EXIT Ordered Sets with CL0s Phase field set to 00t at the beginning of an RS-FEC block after detecting LFPS
12. Verify that the first CL0s\_EXIT Ordered Set sent within tTrainingTransition time from the LFPS
13. Link Partner will stop LFPS, move to Electrical Idle and then will send Gen 4 TS1
14. Verify that the PUT sends 24 CL0s\_EXIT Ordered Sets with CL0s Phase field set to 01t at the beginning of an RS-FEC block after detecting Gen 4 TS1 with Indication field set to 2h
15. Verify that the first CL0s\_EXIT Ordered Set sent within (tWarmUpCL0s + tTrainingTransition) time from the Gen 4 TS1 with Indication field set to 2h
16. Link Partner will stop Gen 4 TS1 and start sending Gen 4 TS2
17. Verify that the PUT sends 24 CL0s\_EXIT Ordered Sets with CL0s Phase field set to 02t at the beginning of an RS-FEC block after detecting Gen 4 TS2 with Indication field set to 4h
18. Verify that the first CL0s\_EXIT Ordered Set sent within tTrainingTransition time from the Gen 4 TS2 with Indication field set to 4h
19. Link Partner will stop Gen 4 TS2 and start sending Gen 4 TS3
20. Verify that the PUT sends 24 CL0s\_EXIT Ordered Sets with CL0s Phase field set to 10t at the beginning of an RS-FEC block after detecting Gen 4 TS3 with Indication field set to 5h
21. Verify that the first CL0s\_EXIT Ordered Set sent within tTrainingTransition time from the Gen 4 TS3 with Indication field set to 5h
22. Link Partner will stop Gen 4 TS3 and start sending Gen 4 TS4 with increasing Counter value.
23. Verify that the PUT transition to CL0 after it received the Gen 4 TS4 with Counter field set to Fh.
24. Verify that the PUT doesn't initiate entry to Low Power state during the above flow.
25. Enable CLx states in the PUT:
  - a. CL2 Enable = 0b
  - b. CL1 Enable = 0b
  - c. CL0s Enable = 1b
26. 26. Enable CLx states in the Link Partner:
  - a. CL2 Enable = 0b
  - b. CL1 Enable = 0b
  - c. CL0s Enable = 1b

## Part 3 – Initiate CL0s Entry by PUT:

27. 27. Enable CLx states in the PUT:
  - a. CL2 Enable = 0b
  - b. CL1 Enable = 1b
  - c. CL0s Enable = 1b
28. 28. Enable CLx states in the Link Partner:
  - a. CL2 Enable = 0b
  - b. CL1 Enable = 0b
  - c. CL0s Enable = 1b
29. 29. Verify that the PUT sends at least 24 CL\_OFF Ordered Sets with index field set to 0 and CLx state field set to 1t.
30. 30. Verify that the PUT sends 102 CL\_OFF Ordered Sets or valid Data Sets
31. 31. If there are Re-timers on the Link repeat the following steps for each Re-timer  
i=1..number of Re-timers:
  - a. Verify that the PUT sends at least 24 CL\_OFF Ordered Sets with index field set to i and CLx state field set to 1t.

- b. Verify that the PUT sends 102 CL\_OFF Ordered Sets or valid Data Sets
- 32. 32. Verify that the PUT is in CL0s (Tx) state
- 33. 33. Verify that transmitter is in electrical idle
- 34. 34. Verify that Lane common mode voltages are maintained

#### Part 4 –Initiate CL0s Exit by PUT

- 35. 35. Send a Read Request to cause the PUT Adapters to exit the CL0s state
- 36. 36. Verify that the PUT sends LFPS until all the following are true:
  - a. PUT sent at least 16 LFPS cycles
  - b. PUT detects CL0s\_EXIT Ordered Set with CL0s Phase field set to 00t
- 37. 37. Verify that the PUT moves to Electrical Idle for tPreData time after the LFPS and then sends Gen 4 TS1 with Indication field set to 2h without SSC.
- 38. 38. Verify that the PUT uses the same TxFFE Preset it used prior to CL0s entry
- 39. 39. Link Partner will send CL0s\_EXIT Ordered Sets with CL0s Phase field set to 01t
- 40. 40. Verify that the PUT sends Gen 4 TS2 with Indication field set to 4h on all enabled transmitters.
- 41. 41. Verify that the first Gen 4 TS2 is sent within tTrainingTransition time after the first CL0s\_EXIT Ordered Set.
- 42. 42. Link Partner will send CL0s\_EXIT Ordered Sets with CL0s Phase field set to 02t
- 43. 43. Verify that the PUT sends Gen 4 TS3 with Indication field set to 5h on all enabled transmitters.
- 44. 44. Verify that the first Gen 4 TS3 is sent within tTrainingTransition time after the first CL0s\_EXIT Ordered Set.
- 45. 45. Link Partner will send CL0s\_EXIT Ordered Sets with CL0s Phase field set to 10t
- 46. 46. Verify that the PUT sends Gen 4 TS4 with Counter field set to 0h on all enabled transmitters.
- 47. 47. Verify that the first Gen 4 TS4 is sent within tTrainingTransition time after the first CL0s\_EXIT Ordered Set.
- 48. 48. Verify that the PUT sends Gen 4 TS4 with increasing value on the Counter field from 1h to Fh
- 49. 49. Verify that the first RS-FEC block in CL0 is De-Skew Block
- 50. 50. Verify that the PUT is in CL0

## TD 4.105 Asymmetric Transition with 3 Receivers Test

*Note: This test only applies to a PUT that supports USB4 Ver. 2.*

- A. Purpose:
  - Verify that the PUT executes the Asymmetric Transitions properly
- B. Asserts:
  -
- C. Test Setups
  - AN\_HOST\_DFP1 (Host)
  - AN\_DEV\_UFP1 (Device)
  - AN\_HUB\_UFP1 (Hub UFP)
  - AN\_HUB\_DFP1 (Hub DFP)
- D. Procedure:

USB4 CV performs the following steps:

### Part 0 - Init

1. Start Analyzer
2. Reset UUT
3. Enumerate RUT
4. Read Logical Layer Error field in LANE\_ADP\_CS\_1 to clear all errors indications
5. Enable Enhanced uni-directional Time Sync Handshakes:
  - a. TSPacketInterval = 16 (HiFi)
  - b. EnableEnhancedUniDirectionalMode = 1

### Part 1 – Transition to Asymmetric Link with 3 receivers

6. Set Target Asymmetric Link in the PUT to 10b
7. Set Target Asymmetric Link in the Link Partner to 01b
8. Set StartAsymmetriFlow in the PUT
- ~~9. Verify that the PUT sends and RS-FEC block with 120 UNBOND Ordered Sets~~
- ~~10.9.~~ Verify that the PUT sends 24 CL\_OFF Ordered Sets with CLx State field set to 1t and Index field set to 0t on Tx1 only.
- ~~11.10.~~ Verify that the PUT sends 102 valid Data Sets or CL\_OFF Ordered Sets on Tx1 only.
- ~~12.11.~~ If there are Re-timers on the Link repeat the following steps for each Re-timer  
i=1..number of Re-timers:
  - a. Verify that the PUT sends at least 24 CL\_OFF Ordered Sets with index field set to i and CLx state field set to 1t on Tx1 only.
  - b. Verify that the PUT sends 102 CL\_OFF Ordered Sets or valid Data Sets on Tx1 only
- ~~13.12.~~ Verify that Tx1 is turned off tTxOff time after sending the last CL\_OFF or valid Data Set.
- ~~14.13.~~ Verify that the PUT sends an LT\_SwitchRx2Tx Transaction
- ~~15.14.~~ Link Partner will respond with LT\_SwitchAck transaction
- ~~16.15.~~ Link partner will send LFPS on its new transmitter
- ~~17.16.~~ Verify that when detecting the LFPS, PUT sends 24 CL0s\_EXIT Ordered Set with CL0s Phase field set to 00t on its active transmitter on RS-FEC block Boundary.
- ~~18.17.~~ Link Partner will send Gen 4 TS1 with Indication field set to 2h.

- 19.18. Verify that the new receiver in the PUT is executing the TxFFE negotiation as described in step 22 in TD 4.5
- 20.19. Verify that the PUT sends 24 CL0s\_EXIT Ordered Sets with CL0s Phase field set to 01t on its active transmitter on RS-FEC block Boundary.
- 21.20. Link Partner will send Gen 4 TS2 with Indication field set to 4h.
- 22.21. Verify that the PUT sends 24 CL0s\_EXIT Ordered Sets with CL0s Phase field set to 02t on its active transmitter on RS-FEC block Boundary.
- 23.22. Link Partner will send Gen 4 TS3 with Indication field set to 5h.
- 24.23. Verify that the PUT sends 24 CL0s\_EXIT Ordered Sets with CL0s Phase field set to 10t on its active transmitter on RS-FEC block Boundary.
- 25.24. Link Partner will send Gen 4 TS4 with Counter field with increasing values from 0h to Fh.
- 26.25. Link Partner will send a De-skew Block on all 3 transmitters.
- 27.26. Verify that the PUT has set the AsymmetricTransitionInProgress bit to 0b.
- 28.27. Verify that the PUT has set the Negotiated Link Width to 001000b
- 29.28. If PUT is a DFP, verify that a Notification Packet with Event Code = ASYM\_LINK is sent upstream.
- 30.29. Read the Adapter State field of the Lane 0 Adapter in both PUT and Link Partner and verify they both in CL0.
- 31.30. If PUT is a DFP, verify that Time Sync Handshakes are resumed.
- 32.31. Read Logical Layer Errors field in LANE\_ADAP\_CS\_1 and verify that it's 00\_0000b

## Part 2 – Transition to Symmetric Link

- 33.32. Set Target Asymmetric Link in the PUT to 00b
- 34.33. Set Target Asymmetric Link in the Link Partner to 00b
- 35.34. Set StartAsymmetricFlow in the Link Partner
- 36.35. Link Partner will send an RS-FEC block with 120 UNBOND Ordered Sets
- 37.36. Link Partner will send 24 CL\_OFF Ordered Sets with CLx State field set to 1t and Index field set to 0t on Tx2 only.
- 38.37. Link Partner will send 102 valid Data Sets or CL\_OFF Ordered Sets on Tx2 only.
- 39.38. If there are Re-timers on the Link, the Link Partner will do the following steps for each Re-timer i=1..number of Re-timers:
  - a. Send at least 24 CL\_OFF Ordered Sets with index field set to i and CLx state field set to 1t on Tx2 only.
  - b. Send 102 CL\_OFF Ordered Sets or valid Data Sets on Tx2 only
- 40.39. Link Partner will turn off Tx2 tTxOff time after sending the last CL\_OFF or valid Data Set.
- 41.40. Link Partner will send an LT\_SwitchRx2Tx Transaction
- 42.41. Verify that the PUT responds with LT\_SwitchAck transaction within tSwitchAck time from receiving the LT\_SwitchRx2Tx
- 43.42. Verify that the PUT sends LFPS on Tx1
- 44.43. Verify that when PUT stops sending LFPS only after detecting CL0s\_EXIT Ordered Set with CL0s Phase field set to 00t on its active receivers on RS-FEC block Boundary.
- 45.44. Verify that the PUT goes to Electrical Idle for tPreData
- 46.45. Verify that the PUT sends Gen 4 TS1 with Indication field set to 2h on its new transmitter.
- 47.46. The Link Partner new receiver will execute the TxFFE negotiation as described in step 22 in TD 4.5
- 48.47. The Link Partner will send 24 CL0s\_EXIT Ordered Sets with CL0s Phase field set to 01t on its active transmitter on RS-FEC block Boundary.
- 49.48. Verify that the PUT sends Gen 4 TS2 with Indication field set to 4h on its new transmitter.



- ~~50~~.~~49~~. The Link Partner will send 24 CL0s\_EXIT Ordered Sets with CL0s Phase field set to 02t on its active transmitter on RS-FEC block Boundary.
- ~~51~~.~~50~~. Verify that the PUT sends Gen 4 TS3 with Indication field set to 5h on its new transmitter.
- ~~52~~.~~51~~. The Link Partner will send 24 CL0s\_EXIT Ordered Sets with CL0s Phase field set to 10t on its active transmitter on RS-FEC block Boundary.
- ~~53~~.~~52~~. Verify that the PUT sends TS4 with Counter field increasing value from 0h to Fh on its new transmitter.
- ~~54~~.~~53~~. Verify that after the TS4 with Counter fields set to Fh, the new transmitter enabled Scrambling and Pre-coding and sends back-to-back DESKEW.0 Ordered Set or Data Sets.
- ~~55~~.~~54~~. Verify that on an RS-FEC Block Boundary, the PUT sends Deskew Block on both its transmitters.
- ~~56~~.~~55~~. If PUT is a DFP, verify that a Notification Packet with Event Code = ASYM\_LINK is sent upstream.
- ~~57~~.~~56~~. Verify that the PUT has set the Negotiated Link Width to 0000010b
- ~~58~~.~~57~~. Read the Adapter State field of the Lane 0 Adapter in both PUT and Link Partner and verify they both in CL0.
- ~~59~~.~~58~~. If PUT is a DFP, verify that Time Sync Handshakes are resumed.
- ~~60~~.~~59~~. Read Logical Layer Errors field in LANE\_ADP\_CS\_1 and verify that it's 00\_0000b

## TD 4.106 Asymmetric Transition with 3 Transmitters Test

*Note: This test only applies to a PUT that supports USB4 Ver. 2.*

- A. Purpose:
  - Verify that the PUT executes the Asymmetric Transitions properly
- B. Asserts:
  -
- C. Test Setups
  - AN\_HOST\_DFP1 (Host)
  - AN\_DEV\_UFP1 (Device)
  - AN\_HUB\_UFP1 (Hub UFP)
  - AN\_HUB\_DFP1 (Hub DFP)
- D. Procedure:

USB4 CV performs the following steps:

### Part 0 - Init

1. Start Analyzer
2. Reset UUT
3. Enumerate RUT
4. Read Logical Layer Error field in LANE\_ADP\_CS\_1 to clear all errors indications
5. Enable Enhanced uni-directional Time Sync Handshakes:
  - a. TSPacketInterval = 16 (HiFi)
  - b. EnableEnhancedUniDirectionalMode = 1

### Part 1 – Transition to Asymmetric Link with 3 transmitters

6. Set Target Asymmetric Link in the PUT to 01b
7. Set Target Asymmetric Link in the Link Partner to 10b
8. Set StartAsymmetriFlow in the Link Partner
- ~~9. Link Partner will send an RS-FEC block with 120 UNBOND Ordered Sets~~
- ~~10.9.~~ Link Partner will send 24 CL\_OFF Ordered Sets with CLx State field set to 1t and Index field set to 0t on Tx1 only.
- ~~11.10.~~ Link Partner will send 102 valid Data Sets or CL\_OFF Ordered Sets on Tx1 only.
- ~~12.11.~~ If there are Re-timers on the Link, the Link Partner will do the following steps for each Re-timer i=1..number of Re-timers:
  - a. Send at least 24 CL\_OFF Ordered Sets with index field set to i and CLx state field set to 1t on Tx1 only.
  - b. Send 102 CL\_OFF Ordered Sets or valid Data Sets on Tx1 only
- ~~13.12.~~ Link Partner will turn off Tx1 tTxOff time after sending the last CL\_OFF or valid Data Set.
- ~~14.13.~~ Link Partner will send an LT\_SwitchRx2Tx Transaction
- ~~15.14.~~ Verify that the PUT responds with LT\_SwitchAck transaction within tSwitchAck time from receiving the LT\_SwitchRx2Tx
- ~~16.15.~~ Verify that the PUT sends LFPS on Tx2
- ~~17.16.~~ Verify that when PUT stops sending LFPS only after detecting CL0s\_EXIT Ordered Set with CL0s Phase field set to 00t on its active receivers on RS-FEC block Boundary.
- ~~18.17.~~ Verify that the PUT goes to Electrical Idle for tPreData

- ~~19.~~18. Verify that the PUT sends Gen 4 TS1 with Indication field set to 2h on its new transmitter.
- ~~20.~~19. The Link Partner new receiver will execute the TxFFE negotiation as described in step 22 in TD 4.5
- ~~21.~~20. The Link Partner will send 24 CL0s\_EXIT Ordered Sets with CL0s Phase field set to 01t on its active transmitter on RS-FEC block Boundary.
- ~~22.~~21. Verify that the PUT sends Gen 4 TS2 with Indication field set to 4h on its new transmitter.
- ~~23.~~22. The Link Partner will send 24 CL0s\_EXIT Ordered Sets with CL0s Phase field set to 02t on its active transmitter on RS-FEC block Boundary.
- ~~24.~~23. Verify that the PUT sends Gen 4 TS3 with Indication field set to 5h on its new transmitter.
- ~~25.~~24. The Link Partner will send 24 CL0s\_EXIT Ordered Sets with CL0s Phase field set to 10t on its active transmitter on RS-FEC block Boundary.
- ~~26.~~25. Verify that the PUT sends TS4 with Counter field increasing value from 0h to Fh on its new transmitter.
- ~~27.~~26. Verify that after the TS4 with Counter fields set to Fh, the new transmitter enabled Scrambling and Pre-coding and sends back-to-back DESKEW.0 Ordered Set or Data Sets.
- ~~28.~~27. Verify that on an RS-FEC Block Boundary, the PUT sends Deskew Block on all its transmitters.
- ~~29.~~28. If PUT is a DFP, verify that a Notification Packet with Event Code = ASYM\_LINK is sent upstream.
- ~~30.~~29. Verify that the PUT has set the Negotiated Link Width to 000100b
- ~~31.~~30. Read the Adapter State field of the Lane 0 Adapter in both PUT and Link Partner and verify they both in CL0.
- ~~32.~~31. If PUT is a DFP, verify that Time Sync Handshakes are resumed.
- ~~33.~~32. Read Logical Layer Errors field in LANE\_ADP\_CS\_1 and verify that it's 00\_0000b

## Part 2 – Transition to Symmetric Link

- ~~34.~~33. Set Target Asymmetric Link in the PUT to 00b
- ~~35.~~34. Set Target Asymmetric Link in the Link Partner to 00b
- ~~36.~~35. Set StartAsymmetriFlow in the PUT
- ~~37. Verify that the PUT sends and RS-FEC block with 120 UNBOND Ordered Sets~~
- ~~38.~~36. Verify that the PUT sends 24 CL\_OFF Ordered Sets with CLx State field set to 1t and Index field set to 0t on Tx2 only.
- ~~39.~~37. Verify that the PUT sends 102 valid Data Sets or CL\_OFF Ordered Sets on Tx2 only.
- ~~40.~~38. If there are Re-timers on the Link repeat the following steps for each Re-timer  
i=1..number of Re-timers:
  - a. Verify that the PUT sends at least 24 CL\_OFF Ordered Sets with index field set to i and CLx state field set to 1t on Tx2 only.
  - b. Verify that the PUT sends 102 CL\_OFF Ordered Sets or valid Data Sets on Tx2 only
- ~~41.~~39. Verify that Tx2 is turned off tTxOff time after sending the last CL\_OFF or valid Data Set.
- ~~42.~~40. Verify that the PUT sends an LT\_SwitchRx2Tx Transaction
- ~~43.~~41. Link Partner will respond with LT\_SwitchAck transaction
- ~~44.~~42. Link partner will send LFPS
- ~~45.~~43. Verify that when detecting the LFPS, PUT sends 24 CL0s\_EXIT Ordered Set with CL0s Phase field set to 00t on its active transmitter on RS-FEC block Boundary.
- ~~46.~~44. Link Partner will send Gen 4 TS1 with Indication field set to 2h.
- ~~47.~~45. Verify that the new receiver in the PUT is executing the TxFFE negotiation as described in step 22 in TD 4.5

- ~~48~~.~~46~~. Verify that the PUT sends 24 CL0s\_EXIT Ordered Sets with CL0s Phase field set to 01t on its active transmitters on RS-FEC block Boundary.
- ~~49~~.~~47~~. Link Partner will send Gen 4 TS2 with Indication field set to 4h.
- ~~50~~.~~48~~. Verify that the PUT sends 24 CL0s\_EXIT Ordered Sets with CL0s Phase field set to 02t on its active transmitters on RS-FEC block Boundary.
- ~~51~~.~~49~~. Link Partner will send Gen 4 TS3 with Indication field set to 5h.
- ~~52~~.~~50~~. Verify that the PUT sends 24 CL0s\_EXIT Ordered Sets with CL0s Phase field set to 10t on its active transmitters on RS-FEC block Boundary.
- ~~53~~.~~51~~. Link Partner will send Gen 4 TS4 with Counter field with increasing values from 0h to Fh.
- ~~54~~.~~52~~. Link Partner will send a De-skew Block on both transmitters.
- ~~55~~.~~53~~. Verify that the PUT has set the AsymmetricTransitionInProgress bit to 0b.
- ~~56~~.~~54~~. If PUT is a DFP, verify that a Notification Packet with Event Code = ASYM\_LINK is sent upstream.
- ~~57~~.~~55~~. Verify that the PUT has set the Negotiated Link Width to 000010b
- ~~58~~.~~56~~. Read the Adapter State field of the Lane 0 Adapter in both PUT and Link Partner and verify they both in CL0.
- ~~59~~.~~57~~. If PUT is a DFP, verify that Time Sync Handshakes are resumed.
- ~~60~~.~~58~~. Read Logical Layer Errors field inLANE\_ADP\_CS\_1 and verify that it's 00\_0000b.

*Note: This test only applies to a PUT that supports Gen 4 speed.*

- A. Purpose:
  - Verify that the PUT executes the Gen 4 Link Recovery Flow properly
- B. Asserts:
  -
- C. Test Setups
  - AN\_HOST\_DFP1 (Host)
  - AN\_DEV\_UFP1 (Device)
  - AN\_HUB\_UFP1 (Hub UFP)
  - AN\_HUB\_DFP1 (Hub DFP)
- D. Procedure:

USB4 CV performs the following steps:

#### Part 0 - Init

1. Start Analyzer
2. Reset UUT
3. Enumerate RUT
4. Enable Enhanced uni-directional Time Sync Handshakes:
  - a. TSPacketInterval = 16 (HiFi)
  - b. EnableEnhancedUniDirectionalMode = 1

#### Part 1 – Gen 4 Link Recovery Initiated by the PUT

5. Enable Gen 4 Recovery Flow in both PUT and Link Partner by setting Enable Gen 4 Link Recovery bit in PORT\_CS\_19 to 1b.
6. Set the Initiate Gen 4 Link Recovery bit in the PUT to 1b.
7. If the PUT is a DFP, verify that it stops sending TSNOS Ordered Sets.
8. Verify that the PUT is not sending any Transport Layer Packets.
9. Verify the PUT sends an ELT\_Recovery Transaction on its Sideband Channel.
10. Link Partner will send an ELT\_Recovery Transaction.
11. Verify the PUT shut down its transmitters within tRecoveryTxOff time from receiving the ELT\_Recovery Transaction.
12. Verify that the PUT starts Lane Initialization from Phase 4 as described in TD 4.5 with the following changes:
  - a. PUT shall use TxFFE Preset from previous Lane Initialization and shall not perform TxFFE negotiation.
13. Verify that the PUT doesn't initiate Disconnect by setting its SBTX low before tRecoveryAbort time past from sending the ELT\_Recovery Transaction.
14. If the PUT is a DFP, verify that it sends a Notification Packet with Event Code = LINK\_RECOVERY when it transitions to CL0
15. Verify that Time Sync Handshakes are resumed after the Gen 4 Link Recovery Flow has ended.

## Part 2 – Gen 4 Link Recovery Initiated by the Link Partner

16. Set the Initiate Gen 4 Link Recovery bit in the Link Partner to 1b.
17. Link Partner will send an ELT\_Recovery Transaction.
18. Verify that the PUT shut down its transmitters within tRecoveryTxOff time from receiving the ELT\_Recovery Transaction.
19. Verify that the PUT sends an ELT\_Recovery Transaction within tRecoveryResponse time from receiving the ELT\_Recovery Transaction.
20. Verify that the PUT starts Lane Initialization from Phase 4 as described in TD 4.5 with the following changes:
  - a. PUT shall use TxFFE Preset from previous Lane Initialization and shall not perform TxFFE negotiation.
21. Verify that the PUT doesn't initiate Disconnect by setting its SBTX low before tRecoveryAbort time past from sending the ELT\_Recovery Transaction.
22. If the PUT is a DFP, verify that it sends a Notification Packet with Event Code = LINK\_RECOVERY when it transitions to CL0
23. Verify that Time Sync Handshakes are resumed after the Gen 4 Link Recovery Flow has ended.

## TD 4.108 Gen 4 TSNOS Coding Test

*Note: This test only applies to a PUT that supports Gen 4 speed.*

- A. Purpose:
  - Verify that the PUT encodes the TSNOS Ordered Sets properly in Gen 4 Link
- B. Asserts:
  -
- C. Test Setups
  - AN\_HOST\_DFP1 (Host)
  - AN\_DEV\_UFP1 (Device)
  - AN\_HUB\_UFP1 (Hub UFP)
  - AN\_HUB\_DFP1 (Hub DFP)
- D. D. Procedure:

USB4 CV performs the following steps:

### Part 0 - Init

1. Start Analyzer
2. Reset UUT
3. Enumerate RUT
4. Enable Enhanced uni-directional Time Sync Handshakes:
  - a. TSPacketInterval = 16 (HiFi)
  - b. EnableEnhancedUniDirectionalMode = 1

### Part 1 – TSNOS Request (DFP)

5. Verify that TSNOS Requests are sent in 16us interval with 100ppm (+/-1%).
  - a. Use Cycles Delay in the TSNOS to calculate the exact time it was sent

### Part 2 – TSNOS Response (UFP)

6. Verify that the TSNOS Response are send with a variance of less than 32ns
  - a. Use Cycles Delay in the TSNOS to calculate the exact time it was sent

## USB4 Mode Tests – Exerciser Required

The tests in this section are performed in USB4 mode where all connected Ports negotiate and enter USB4 operation as described in the USB Type-C Specification and the USB PD Specification. The Sideband Channel operates as a USB4 Sideband Channel.

Unless specified otherwise, the tests in this section are performed on all Ports of a UUT. The tests are performed at the highest speed that the UUT supports. Lanes are bonded and RS-FEC is enabled.

Unless otherwise noted, a test will timeout if it takes more than 500ms to go from one step to the next step. It is a test failure if a test times out.

### Background Checks

#### Sideband Channel Background Check

This test is performed by the Exerciser in conjunction with all of the Sideband Channel Tests.

1. Parse each LT Transaction and verify that it consists of the following symbols in the following order:  
(4.1.1.2.1#1)

- a. A DLE symbol (FEh)
- b. A LSE symbol
- c. A CLSE symbol

2. Parse the LSE Symbol in each LT Transaction and verify that:

- a. Bits [7:6] (*StartLT*) are set to 10b (4.1.1.2.1#4)
- b. Bit 5 (*LSELane*) is 0 for an LT\_LRoff Transaction (4.1.1.2.1#3)
- c. Bit 4 is reserved (0b) (1.7#5)
- d. Bits [3:0] (*LSESymbol*) do not contain reserved values (1.7#1)

*Note: Defined LSESymbol values are 0000b (LT\_Fall), 0010b (LT\_Resume), and 0011b (LT\_LRoff)*

3. Parse each AT Transaction and verify that it consists of the following symbols in the following order:  
(4.1.1.2.2#1)

- a. A DLE symbol (FEh)
- b. A STX symbol
- c. A DLE symbol (FEh)
- d. No more than 66 Data Symbols (4.1.1.2.2#2)
- e. 2 CRC Symbols (Low and High) with correct CRC (4.1.1.2.4#5, 4.1.1.2.4#6, 4.1.1.2.4#7, 4.1.1.2.4#8, 4.1.1.2.4#9)
- f. An ETX symbol (40h)

4. For each AT Command:

- a. Parse the STX Symbol and verify that:
  - i. Bits [7:6] (*StartAT*) are 00b (4.1.1.2.2#8)
  - ii. Bit 5 is reserved (0b) (1.7#5)
  - iii. Bit 4 (*Responder*) is 0b (4.1.1.2.2#7)
  - iv. Bit 3 (*Bounce*) is set to 0b (4.1.1.2.2#6)
  - v. Bit 2 (*Recipient*) is 1b (4.1.1.2.2#5)
  - vi. Bit 1 (*ReturnBounce*) is set to 0b (4.1.1.2.2#4)



- b. Parse the Data Symbols and verify that: (4.1.1.3.1#1)
      - i. The REG symbol does not contain the values 2 to 7, 10 to 11, 14, or 128 to 255
      - ii. The LEN symbol does not contain a value greater than 64 (4.1.1.3.1#2)
      - iii. If WnR=0, there is no COMMAND\_DATA
      - iv. If WnR=1b, the COMMAND\_DATA is the same length as in the LEN field
- 5. For each AT Response:
  - a. Parse the STX Symbol and verify that:
    - i. Bits [7:6] (*StartAT*) are 00b (4.1.1.2.2#8)
    - ii. Bit 5 is reserved (0b) (1.7#5)
    - iii. Bit 4 (*Responder*) is 0b (4.1.1.2.2#7)
    - iv. Bit 3 (*Bounce*) is set to 0b (4.1.1.2.2#6)
    - v. Bit 2 (*Recipient*) is 1b (4.1.1.2.2#5)
    - vi. Bit 1 (*ReturnBounce*) is set to 0b (4.1.1.2.2#4)
  - b. Parse the Data Symbols and verify that they consist of the following symbols in the following order: (4.1.1.3.1#2)
    - i. A REG symbol does not contain the values 2 to 7, 10 to 11, 14, or 128 to 255
    - ii. A LEN symbol does not contain a value greater than 64 (4.1.1.3.1#2)
    - iii. If WnR=0b, RESPONSE\_DATA is the same length as in the LEN field (unless test specifies otherwise)
    - iv. If WnR=1n, RESPONSE\_DATA is 00h (unless test specified otherwise)
  - c. Verify that the value in the LEN field is not greater than 64 (4.1.1.3.1#2)
- 6. When the PUT receives an AT Command with the Recipient bit set to 1b, verify that the PUT responds with an AT Response (unless the test specifies otherwise). (4.1.1.2.2#9)
- 7. Parse each Broadcast RT Transaction and verify that it consists of the following symbols in the following order: (4.1.1.2.3.1#1)
  - a. A DLE symbol (FEh)
  - b. A STX symbol
  - c. Two Link Parameters symbols
  - d. 2 CRC Symbols (Low and High) with correct CRC (4.1.1.2.4#5, 4.1.1.2.4#6, 4.1.1.2.4#7, 4.1.1.2.4#8, 4.1.1.2.4#9)
  - e. A DLE symbol (FEh)
  - f. An ETX symbol (40h)
- 8. Parse the STX Symbol for a Broadcast RT Transaction and verify that:
  - a. *Index* = 0 (4.1.1.2.3.1#4)
  - b. *CmdNotResp*=1b (4.1.1.2.3.1#5)
- 9. Parse Byte 2 of a Broadcast RT Transaction and verify that:
  - a. Bits [7:5] are 0 (reserved) (1.7#5)
  - b. Bit 4 (*TBtCompatibleSpeed*) is 0b (4.1.1.2.3.1#6)
  - c. Bit 1 (reserved) is 0b (1.7#5)
  - d. Bit 0 (*USB4*) is 1b (4.1.1.2.3.1#7)
- 10. Parse each Addressed RT Transaction and verify that it consists of the following symbols in the following order: (4.1.1.2.3.2#1)
  - a. A DLE symbol (FEh)
  - b. A STX symbol
  - c. No more than 66 Data Symbols (4.1.1.2.3.2#2)
  - d. 2 CRC Symbols (Low and High) with correct CRC (4.1.1.2.4#5-#9)
  - e. A DLE symbol (FEh)
  - f. An ETX symbol (40h)

11. Parse each RT Command and verify that: (4.1.1.3.1#1)
  - a. The REG symbol does not contain the values 2 to 7, 10 to 11, 14, or 128 to 255
  - b. The LEN symbol does not contain a value greater than 64
  - c. If WnR=0, there is no COMMAND\_DATA
  - d. If WnR=1b, the COMMAND\_DATA is the same length as in the LEN field
12. Parse each RT Response and verify that it consists of the following symbols in the following order: (4.1.1.3.1#2)
  - a. The REG symbol does not contain the values 2 to 7, 10 to 11, 14, or 128 to 255
  - b. The LEN symbol does not contain a value greater than 64 (4.1.1.3.1#2)
  - c. If WnR=0b, RESPONSE\_DATA is the same length as in the LEN field (unless test specifies otherwise)
  - d. If WnR=1n, RESPONSE\_DATA is 00h (unless test specified otherwise)
13. Verify that the PUT sends an AT Response within tCmdResponse (50ms) of receiving an AT Command. (4.1.1.2.5.1#1)
14. Verify that the PUT sends an Addressed RT Response within tCmdResponse (50ms) of receiving an Addressed RT Command. (4.1.1.2.5.2#1)

### Lane 0/Lane 1 Background Check

This test is performed by the Exerciser in conjunction with all of the Lane 0/Lane 1 Tests.

1. Parse each TS1 and TS2 Ordered Set and verify that bits 31:29 (Rsvd) are 0. (4.2.1.3.5#6)
2. When an Adapter transitions to the CL0 state and Lanes are not bonded, verify that the first bytes transmitted after the last TS2 Ordered Set are either a Transport Layer Packet header or an Ordered Set that is not SLOS, TS1, or TS2. (4.4.1#1)
3. When an Adapter transitions to the CL0 state and Lanes are bonded, verify that the first bytes transmitted after the last TS2 Ordered Set are a de-skew Ordered Set followed by either a Transport Layer Packet header, an Idle Packet or any Ordered Set other than SLOS, TS1 or TS2. (4.4.1#2)
4. When operating with a Dual-lane Link, verify that, if one Lane transitions to Training State, other Lane also transitions to training state (4.2.2.2#8)

## Test Descriptions

### TD 4.004 Command Timeout Test

- A. Purpose:
- Verify that the PUT records a Transaction timeout in SB Register Space
  - Verify that the PUT waits tATTimeout before timing out an AT Command
  - Verify that the PUT only sends one AT Command or Addressed RT Command at a time
- B. Asserts:
- 4.1.1.2.5#3
  - 4.1.1.2.5.1#3
  - 4.1.1.2.5.2#2
  - 4.1.1.3.2#21, 4.1.1.3.2#24
- C. Test Setups
- EX\_HOST\_DFP1 (Host)
  - EX\_DEV\_UFP1 (Device)
  - EX\_HUB\_UFP1 (Hub UFP)
  - EX\_HUB\_DFP1 (Hub DFP)
- D. Repetitions:
- Repeat with AT Transactions that target the Link Partner (*Target* = 001b)
  - Repeat with Addressed RT Transactions with invalid index (*Target* = 010b, *Index* = 7)
- E. Background Check:
- Sideband Channel Background Check
- F. Procedure:

*Note: When performing this test on an UFP, the exerciser performs both the test steps that are defined “Upstream of the UUT” and the test steps that are defined “On the PUT”. When this test is performed on a DFP, USB4 CV performs the tests steps that are defined “Upstream of the UUT” and the Exerciser performs the test steps that are defined “On the PUT”.*

#### Upstream of the UUT:

##### Part 0 - Setup

1. Reset UUT
2. Enumerate UUT Router
3. Initiate Lane Bonding
4. Wait for Lane Bonding to complete
5. Configure the Exerciser to not respond to any AT or RT Commands from the PUT

##### Part 1 – Write Command

6. Initiate a Write Command from the PUT by writing the following to the USB4 Port Capability in PUT Configuration Space:
  - a. *Target* = see repetitions
  - b. If sending an Addressed RT Transaction, *Re-Timer Index* = 7
  - c. *Address* = Register 9 (Metadata)
  - d. *Length* = 4

- e. *WnR* = 1 (Write)
- f. *Data DW* = FFFF FFFFh
- 7. Set the *Pending* bit in the USB4 Port Capability in PUT Configuration Space to 1b
- 8. Wait 1 second.
- 9. Verify that the PUT sets the *Pending* bit to 0b (4.1.1.3.2#24)
- 10. Read the *No Response* field from the USB4 Port Capability in PUT Configuration Space:
  - a. *Length*
  - b. *No Response*
  - c. *Result Code*
- 11. Verify that *No Response* = 1 (4.1.1.3.2#21)

USB4 CV does the following:

#### Part 2 – Parse Exerciser Trace

- 12. Read the trace file from the Exerciser
- 13. Parse the trace file and verify the following:
  - a. PUT did not resend the Write Command or send another AT Command or Addressed RT Command until after the Write Command timed out (4.1.1.2.5#3)
  - b. If Write Command is an AT Command, timeout = tATTimeout (4.1.1.2.5.1#3)
  - c. If Write Command is an Addressed RT Command, timeout = tRTTimeout (4.1.1.2.5.2#2)

## TD 4.010 Gen 2/3 CL2 Test (No Re-timers on the Link)

*Note: This test only applies to Ports that do not contain any On-Board Re-timers.*

*Note: This test is performed with a Passive Cable to avoid introducing re-timers on the Link. The test is performed simultaneously for both the Lane 0 Adapter and the Lane 1 Adapter of the Port being tested.*

*Note: This test does not apply at Gen 4 speed. It is performed at Gen 3 speed if supported by the UUT. Otherwise the test is performed at Gen 2 speed.*

- A. Purpose:
  - Verify that the PUT enters CL2 state correctly when there are no Re-timers on the Link
  - Verify that the PUT exits CL2 state correctly when there are no Re-timers on the Link
- B. Asserts:
  - 4.2.1.6.1#3, 4.2.1.6.1#6
  - 4.2.1.6.2#1, 4.2.1.6.2#7, 4.2.1.6.2#10, 4.2.1.6.2#13, 4.2.1.6.2#14
  - 4.2.1.6.3#1
  - 4.2.1.6.5.2#1, 4.2.1.6.5.2#2-6, 4.2.1.6.5.2#8-32
- C. Test Setups
  - EX\_HOST\_DFP1 (Host)
  - EX\_DEV\_UFP1 (Device)
  - EX\_HUB\_UFP1 (Hub UFP)
  - EX\_HUB\_DFP1 (Hub DFP)
- D. Repetitions:
  - Repeat with:
    - Exerciser sends CL2\_REQ after the PM Secondary bit is configured
    - Exerciser sends CL2\_REQ after receiving the first CL2\_REQ from the UUT
    - Exerciser does not send CL2\_REQ
  - Repeat with:
    - EXIT\_TIME = tEnterLFPS1
    - EXIT\_TIME = 30 seconds
- E. Background Check:
  - Gen 2/Gen 3 Gen 2/Gen 3 Lane 0/Lane 1 Background Check
- F. Procedure:

USB4 CV performs the following steps:

### Part 0 – Setup

1. Reset UUT
2. Enumerate UUT Router
3. Initiate Lane Bonding
4. Wait for Lane Bonding to complete
5. Read the *CL2 Support* bit in the PUT
6. Verify that the *CL2 Support* bit matches the capabilities indicated in the VIF
7. Do not enable Bi-Directional Time Sync Handshakes
8. Configure the PM Secondary:
  - a. If the PUT is the UFP, set the *PM Secondary* bit to 1b in the PUT and to 0b in the Exerciser
  - b. If the PUT is a DFP, set the *PM Secondary* bit to 0b in the PUT and to 1b in the Exerciser
9. Enable CLx states in the PUT (if supported) and in the Exerciser:
  - a. *CL2 Enable* = 1b

- b. *CL1 Enable* = 1b
  - c. *CL0s Enable* = 1b
- 10. If both the PUT and Exerciser send CL2\_REQ Ordered Sets at the same time:
  - a. If PUT is not the PM Secondary, perform Part 1
  - b. Else, perform Part 2
- 11. If the Exerciser sends CL2\_REQ Ordered Sets before the PUT:
  - a. If PUT does not support CL2:
    - i. Verify that the PUT sends CL\_NACK Ordered Sets (4.2.1.6.3#1)
    - ii. Perform Part 1
  - b. If PUT sends CL\_NACK Ordered Sets, perform Part 1
  - c. If PUT sends CL2\_ACK Ordered Sets, perform Part 2
- 12. If the PUT sends CL2\_REQ Ordered Sets before the Exerciser:
  - a. If Exerciser sends CL\_NACK Ordered Sets, perform Part 3
  - b. If Exerciser sends CL2\_ACK Ordered Sets, perform Part 4
- 13. If neither send CL2\_REQ Ordered Sets, retry test (stop after 5 attempts)

#### Part 1 – PUT Sends CL\_NACK

- 14. If PUT sent CL2\_REQ Ordered Sets and PM Secondary bit in PUT is 0b, verify that the PUT continues to send CL\_NACK Ordered Sets until last CL2\_REQ Ordered Set is sent (4.2.1.6.2#7)
- 15. Else, verify that:
  - a. The PUT sends 10-40 CL\_NACK Ordered Sets (4.2.1.6.2#13)
  - b. The first CL\_NACK Ordered Set is sent no longer than (tCL0sEntry + tCL0sExit) time after the PUT receives the last CL2\_REQ (4.2.1.6.2#13)
- 16. Parse each CL\_NACK Ordered Set and verify that bits 9:0 (SCR) in the payload are 00 1111 0010b (4.2.1.6.1#6)
- 17. Verify that the PUT is in CL0 state (4.2.1.6.2#14)

#### Part 2 – PUT Sends CL2\_ACK

- 18. Verify that the PUT sends the CL2\_ACK Ordered Set 375 times (4.2.1.6.2#10)

*Note: It is possible that some CL2\_ACK Ordered Sets may not be detected as the Link enters low power state. Because of this, it is not a failure as long as 350 or more CL2\_ACK Ordered Sets are detected.*

*Note: It is not a failure if the PUT sends more than 375 CL2\_ACK Ordered Sets.*

- 19. Parse each CL2\_ACK Ordered Set and verify that bits 9:0 (SCR) in the payload are 00 1111 0010b (4.2.1.6.1#3)
- 20. Perform Part 5

#### Part 3 – Exerciser Sends CL\_NACK

- 21. Verify that the PUT sends back-to-back CL2\_REQ Ordered Set until it receives CL\_NACK Ordered Sets (4.2.1.6.2#1)
- 21-22. Exerciser continues to send CL\_NACK as long as it receives CL2\_REQ Ordered Sets, after CL2\_REQ are not detected it will move to next step.
- 22-23. Wait 1000 ns for the PUT to stop sending CL2\_REQ Ordered Sets
- 23-24. Verify that the PUT does not send another CL2\_REQ Ordered Set or CL1\_REQ Ordered Set for at least tCLxRetry (4.2.1.6.2#20)
- 24-25. PUT Adapters are in CL0 state (4.2.1.6.2#21)

#### Part 4 – Exerciser Sends CL2\_ACK

~~25:26.~~ Verify that the PUT sends back-to-back CL2\_REQ Ordered Sets until it receives CL2\_ACK Ordered Sets (4.2.1.6.2#1)

~~26:27.~~ Verify that the PUT sends 375 CL\_OFF Ordered Sets (4.2.1.6.2#17)

*Note: It is possible that some CL2\_OFF Ordered Sets may not be detected as the Link enters low power state. Because of this, it is not a failure as long as 350 or more CL2\_OFF Ordered Sets are detected.*

~~27:28.~~ Verify that the first CL\_OFF Ordered Set is sent within tCLxResponse after getting the CL2\_ACK Ordered Sets (4.2.1.6.2#18)

~~28:29.~~ Verify that the PUT Adapters are in the CL2 state (4.2.1.6.2#25)

~~29:30.~~ Perform Part 5

#### Part 5 – CL2 Exit

~~30:31.~~ Wait EXIT\_TIME time after detecting that the PUT transitioned to CL2 state (see repetitions)

~~31:32.~~ Tell the Exerciser to initiate exit from CL2 state by sending LFPS

~~32:33.~~ Verify that the PUT does the following:

- a. Sends an LFPS burst on the Lane for at least 5 LFPS cycles (4.2.1.6.5.2#8)
- b. Does not send LFPS for more than tLFPSDuration (4.2.1.6.5.2#8)
- c. Sends the first LFPS within tWarmUpCL2 after receiving the first LFPS cycle (4.2.1.6.5.2#8)
- d. Starts transmitting SLOS on the Lane (4.2.1.3.1#3, 4.2.1.6.5.2#10, 4.2.1.6.5.2#12)

~~33:34.~~ Verify that the PUT transitions to CL0 state (4.2.1.4.1#1)

## TD 4.011 Gen 2/3 CL2 Test (Re-timers on the Link)

*Note: This test applies to Ports that contain On-Board Re-timers as well as Ports that do not.*

*Note: This test is performed with an Active Cable that contains Cable Re-Timers in order to add re-timers to the Link. The Active Cable must support CLx states. The test is performed simultaneously for both the Lane 0 Adapter and the Lane 1 Adapter of the Port being tested.*

*Note: This test does not apply at Gen 4 speed. It is performed at Gen 3 speed if supported by the UUT. Otherwise the test is performed at Gen 2 speed.*

- A. Purpose:
  - Verify that the PUT enters CL2 state correctly when there are Re-timers on the Link
  - Verify that the PUT exits CL2 state correctly when there are Re-timers on the Link
- B. Asserts:
  - 4.2.1.3.1#3
  - 4.2.1.6.1#3, 4.2.1.6.1#6
  - 4.2.1.6.1.2#9, 4.2.1.6.1.2#10
  - 4.2.1.6.2#1, 4.2.1.6.2#7, 4.2.1.6.2#10, 4.2.1.6.2#13, 4.2.1.6.2#14
  - 4.2.1.6.3#1
  - 4.2.1.6.5.3#9-45, 4.2.1.6.5#48
  - 4.2.4.2#1rt
  - 4.2.4.3.2.1#1rt, 4.2.4.3.2.1#4rt, 4.2.4.3.2.1#5rt
  - 4.2.4.3.2.3#4rt
  - 4.2.4.3.3#2rt
- C. Test Setups
  - EX\_HOST\_DFP1 (Host)
  - EX\_DEV\_UFP1 (Device)
  - EX\_HUB\_UFP1 (Hub UFP)
  - EX\_HUB\_DFP1 (Hub DFP)
- D. Repetitions:
  - Repeat with:
    - Exerciser sends CL2\_REQ after the PM Secondary bit is configured
    - Exerciser sends CL2\_REQ after receiving the first CL2\_REQ from the UUT
    - Exerciser does not send CL2\_REQ
  - Repeat with:
    - EXIT\_TIME = tEnterLFPS1
    - EXIT\_TIME = 30 seconds
- E. Background Check:
  - Gen 2/Gen 3 Gen 2/Gen 3 Lane 0/Lane 1 Background Check
- F. Procedure:

USB4 CV performs the following steps:

### Part 0 – Setup

1. Reset UUT
2. Enumerate UUT Router
3. Initiate Lane Bonding
4. Read the *CL2 Support* bit in the PUT
5. Verify that the *CL2 Support* bit matches the capabilities indicated in the VIF
6. Do not enable Bi-Directional Time Sync Handshakes
7. Configure the PM Secondary



- a. If the PUT is the UFP, set the *PM Secondary* bit to 1b in the PUT and to 0b in the Exerciser
  - b. If the PUT is a DFP, set the *PM Secondary* bit to 0b in the PUT and to 1b in the Exerciser
8. Enable CLx states in the PUT (if supported) and in the Exerciser:
  - a. *CL2 Enable* = 1b
  - b. *CL1 Enable* = 1b
  - c. *CL0s Enable* = 1b
9. If both the PUT and Exerciser send CL2\_REQ Ordered Sets at the same time:
  - a. If PUT is not the PM Secondary, perform Part 1
  - b. Else, perform Part 2
10. If the Exerciser sends CL2\_REQ Ordered Sets before the PUT:
  - a. If PUT does not support CL2:
    - i. Verify that the PUT sends CL\_NACK Ordered Sets (4.2.1.6.3#1)
    - ii. Perform Part 1
  - b. If PUT sends CL\_NACK Ordered Sets, perform Part 1
  - c. If PUT sends CL2\_ACK Ordered Sets, perform Part 2
11. If the PUT sends CL2\_REQ Ordered Sets before the Exerciser:
  - a. If Exerciser sends CL\_NACK Ordered Sets, perform Part 3
  - b. If Exerciser sends CL2\_ACK Ordered Sets, perform Part 4
12. If neither send CL2\_REQ Ordered Sets, retry test (stop after 5 attempts)

#### Part 1 – PUT Sends CL\_NACK

13. If PUT sent CL2\_REQ Ordered Sets and the PM Secondary bit in PUT is 0b, verify that the PUT continues to send CL\_NACK Ordered Sets until last CL2 REQ Ordered Set is sent (4.2.1.6.2#7)
14. Else, verify that:
  - a. The PUT sends 16 CL\_NACK Ordered Sets (4.2.1.6.2#13)
  - b. The first CL\_NACK Ordered Set is sent no longer than (tCL0sEntry + tCL0sExit) time after the PUT receives the last CL2\_REQ (4.2.1.6.2#13)
15. Parse each CL\_NACK Ordered Set and verify that bits 9:0 (SCR) in the payload are 00 1111 0010b (4.2.1.6.1#6)
16. Verify that the PUT is in CL0 state (4.2.1.6.2#14)

#### Part 2 – PUT Sends CL2\_ACK

17. Verify that the PUT sends CL2\_ACK Ordered Sets 375 times (4.2.1.6.2#10)

*Note: It is not a failure if the PUT sends more than 375 CL2\_ACK Ordered Sets*

18. Parse each CL2\_ACK Ordered Set and verify that bits 9:0 (SCR) in the payload are 00 1111 0010b (4.2.1.6.1#3)
- 19.
20. Perform Part 5

#### Part 3 – Exerciser Sends CL\_NACK

21. Verify that the PUT sends back-to-back CL2\_REQ Ordered Sets until it receives CL\_NACK Ordered Sets (4.2.1.6.2#1)
- 24-22. Exerciser continues to send CL\_NACK as long as it receives CL2\_REQ Ordered Sets, after CL2\_REQ are not detected it will move to next step.

- 22:23. Verify that the PUT does not send another CL2\_REQ Ordered Set or CL1\_REQ Ordered Set for at least tCLxRetry (4.2.1.6.2#20)
- 23:24. Verify that the PUT Adapters are in CL0 state (4.2.1.6.2#21)

#### Part 4 – Exerciser Sends CL2\_ACK

- 24:25. Verify that the PUT sends back-to-back CL2\_REQ Ordered Sets until it receives CL2\_ACK Ordered Sets (4.2.1.6.2#1)
- 25:26. Verify that the PUT sends 375 CL\_OFF Ordered Sets (4.2.1.6.2#17)
- 26:27. Verify that the first CL\_OFF Ordered Set is sent within tCLxResponse after getting the CL2\_ACK (4.2.1.6.2#18)
- 27:28. Verify that the PUT Adapters are in the CL2 state (4.2.1.6.2#25)
- 28:29. Perform Part 5

#### Part 5 – CL2 Exit

- 29:30. Wait EXIT\_TIME time after detecting that the PUT transitioned to CL2 state (see repetitions)
- 30:31. Tell the Exerciser to initiate exit from CL2 state by sending LFPS
- 31:32. Verify that the PUT does the following:
- Sends a LFPS burst on the Lane for at least 5 LFPS cycles (4.2.1.6.5.3#9)
    - If PUT contains On-Board Re-timers, LFPS is sent for at least 5 LFPS cycles (4.2.4.3.2.1#1rt)
  - Does not send the LFPS burst for more than tLFPSDuration (4.2.1.6.5.3#9)
  - Sends the first LFPS within tWarmUpCL2 after receiving the first LFPS cycle (4.2.1.6.5.3#9)
  - Transmits Ordered Sets as follows:
    - If PUT does not contain On-Board Re-timers, it starts transmitting SLOS on the Lane (4.2.1.6.5.3#11)
    - If PUT contains On-Board Re-timers, it starts transmitting CL\_WAKE1.X Ordered Set Symbols (4.2.4.3.2.1#5rt)
  - Upon reception of 3 consecutive and identical CL\_WAKE1.X Ordered Sets, starts transmitting CL\_WAKE2.X Ordered Sets on the Lane (4.2.1.6.5#48, 4.2.1.6.5.3#13)
    - CL\_WAKE2.X from PUT are not scrambled (4.2.1.6.1.2#9)
    - PUT does not send any partial CL\_WAKE2.X (4.2.1.6.1.2#10)
  - If the PUT receives 7 back-to-back CL\_WAKE2.X Ordered Sets, it transitions to Training.LOCK1 substate (4.2.1.3.1#3, 4.2.1.6.5.3#14)
  - If the PUT receives 7 back-to-back SLOS Symbols, it transitions to Training.LOCK1 substate (4.2.1.3.1#3, 4.2.1.6.5.3#14)
  - 
  - If PUT contains On-Board Re-timers, verify that it stops sending CL\_WAKE1.X Ordered Set Symbols (4.2.4.3.2.3#4rt)
- 32:33. Verify that the PUT transitions to CL0 state

#### TD 4.012 Gen 2/3 CL1 Test (No Re-timers on the Link)

*Note: This test only applies to Ports that do not contain any On-Board Re-timers.*

*Note: This test is performed with a Passive Cable to avoid introducing re-timers on the Link. The test is performed simultaneously for both the Lane 0 Adapter and the Lane 1 Adapter of the Port being tested.*

*Note: This test does not apply at Gen 4 speed. It is performed at Gen 3 speed if supported by the UUT. Otherwise the test is performed at Gen 2 speed.*

- A. Purpose:
  - Verify that the PUT enters CL1 state correctly when there are no Re-timers on the Link
  - Verify that the PUT exits CL1 state correctly when there are no Re-timers on the Link
- B. Asserts:
  - 4.2.1.6.1#4, 4.2.1.6.1#6
  - 4.2.1.6.2#1, 4.2.1.6.2#7, 4.2.1.6.2#11, 4.2.1.6.2#13, 4.2.1.6.2#14, 4.2.1.6.2#30
  - 4.2.1.6.3#16
  - 4.2.1.6.4#2
  - 4.2.1.6.5.2#1, 4.2.1.6.5.2#2-6, 4.2.1.6.5.2#8-32
- C. Test Setups
  - EX\_HOST\_DFP1 (Host)
  - EX\_DEV\_UFP1 (Device)
  - EX\_HUB\_UFP1 (Hub UFP)
  - EX\_HUB\_DFP1 (Hub DFP)
- D. Repetitions:
  - Repeat with:
    - Exerciser sends CL1\_REQ after the PM Secondary bit is configured
    - Exerciser sends CL1\_REQ after receiving the first CL1\_REQ from the UUT
    - Exerciser does not send CL1\_REQ
  - Repeat with:
    - EXIT\_TIME = tEnterLFPS1
    - EXIT\_TIME = 30 seconds
- E. Background Check:
  - Gen 2/Gen 3 Gen 2/Gen 3 Lane 0/Lane 1 Background Check
- F. Procedure:

USB4 CV performs the following steps:

##### Part 0 – Setup

1. Reset UUT
2. Enumerate UUT Router
3. Initiate Lane Bonding
4. Read the *CLI Support* bit in the PUT
5. Verify that the *CLI Support* bit matches the capabilities indicated in the VIF
6. Do not enable Bi-Directional Time Sync Handshakes
7. Configure the PM Secondary
  - a. If the PUT is the UFP, set the *PM Secondary* bit to 1b in the PUT and to 0b in the Exerciser
  - b. If the PUT is a DFP, set the *PM Secondary* bit to 0b in the PUT and to 1b in the Exerciser

8. Enable CLx states in the PUT (if supported) and in the Exerciser:
  - a. *CL2 Enable* = 0b
  - b. *CL1 Enable* = 1b
  - c. *CL0s Enable* = 1b
9. If both the PUT and Exerciser send CL1\_REQ Ordered Sets at the same time:
  - a. If PUT is not the PM Secondary, perform Part 1
  - b. Else, perform Part 2
10. If the Exerciser sends CL1\_REQ Ordered Sets before the PUT:
  - a. If PUT does not support CL1:
    - i. Verify that the PUT sends CL\_NACK Ordered Sets (4.2.1.6.3#16)
    - ii. Perform Part 1
  - b. If PUT sends CL\_NACK Ordered Sets, perform Part 1
  - c. If PUT sends CL1\_ACK Ordered Sets, perform Part 2
11. If the PUT sends CL1\_REQ Ordered Sets before the Exerciser:
  - a. If Exerciser sends CL\_NACK Ordered Sets, perform Part 3
  - b. If Exerciser sends CL1\_ACK Ordered Sets, perform Part 4
12. If neither send CL1\_REQ Ordered Sets, retry test (stop after 5 attempts)

#### Part 1 – PUT Sends CL\_NACK

13. If the PUT sends CL1\_REQ Ordered Sets and the PM Secondary bit in the PUT is 0b, verify that the PUT continues to send CL\_NACK Ordered Sets until last CL1\_REQ Ordered Set is sent (4.2.1.6.2#7)
14. Else, verify that:
  - a. The PUT sends 10-40 CL\_NACK Ordered Sets (4.2.1.6.2#13)
  - b. The first CL\_NACK Ordered Set is sent no longer than (*tCL0sEntry* + *tCL0sExit*) time after the PUT receives the last CL1\_REQ (4.2.1.6.2#13)
15. Parse each CL\_NACK Ordered Set and verify that bits 9:0 (SCR) in the payload are 00 1111 0010b (4.2.1.6.1#6)
16. Verify that the PUT is in CL0 state (4.2.1.6.2#14)

#### Part 2 – PUT Sends CL1\_ACK

17. Verify that the PUT sends CL1\_ACK Ordered Sets 375 times (4.2.1.6.2#11)

*Note: It is possible that some CL1\_ACK Ordered Sets may not be detected as the Link enters low power state. Because of this, it is not a failure as long as 350 or more CL1\_ACK Ordered Sets are detected.*

*Note: It is not a failure if the PUT sends more than 375 CL1\_ACK Ordered Sets*

18. Parse each CL1\_ACK Ordered Set and verify that bits 9:0 (SCR) in the payload are 00 1111 0010b (4.2.1.6.1#4)
19. Perform Part 5

#### Part 3 – Exerciser Sends CL\_NACK

20. Verify that the PUT sends back-to-back CL1\_REQ Ordered Sets until it receives CL\_NACK Ordered Sets (4.2.1.6.2#1)
- 20;21. Exerciser continues to send CL\_NACK as long as it receives CL1\_REQ Ordered Sets, after CL2\_REQ are not detected it will move to next step.
- 24;22. Wait 1000 ns for the PUT to stop sending CL1\_REQ Ordered Sets

- ~~22-23.~~ Verify that the PUT does not send another CL2\_REQ Ordered Set or CL1\_REQ Ordered Set for at least tCLxRetry (4.2.1.6.2#20)
- ~~23-24.~~ Verify that the PUT Adapters are in CL0 state (4.2.1.6.2#21)

#### Part 4 – Exerciser Sends CL1\_ACK

- ~~24-25.~~ Verify that the PUT sends back-to-back CL1\_REQ Ordered Sets until it receives CL1\_ACK Ordered Sets (4.2.1.6.2#1)
- ~~25-26.~~ Verify that the PUT sends 375 CL\_OFF Ordered Sets (4.2.1.6.2#17)

*Note: It is possible that some CL\_OFF Ordered Sets may not be detected as the Link enters low power state. Because of this, it is not a failure as long as 350 or more CL\_OFF Ordered Sets are detected.*

- ~~26-27.~~ Verify that the first CL\_OFF Ordered Set is sent within tCLxResponse after getting the CL1\_ACK Ordered Sets (4.2.1.6.2#18)
- ~~27-28.~~ Verify that the PUT Adapters are in the CL1 state (4.2.1.6.2#26)
- ~~28-29.~~ Perform Part 5

#### Part 5 – CL1 Exit

- ~~29-30.~~ Wait EXIT\_TIME time after detecting that the PUT transitioned to CL1 state (see repetitions)
- ~~30-31.~~ Tell the Exerciser to initiate exit from CL1 state by sending LFPS
- ~~31-32.~~ If the Exerciser initiated CL1 exit, verify that the PUT does the following:
- Sends an LFPS burst on the Lane for at least 5 LFPS cycles (4.2.1.6.5.2#8)
  - Does not send LFPS for more than tLFPSDuration (4.2.1.6.5.2#8)
  - Sends the first LFPS within tWarmUpCL1 after receiving the first LFPS cycle (4.2.1.6.5.2#8)
  - Starts transmitting SLOS on the Lane (4.2.1.3.1#3, 4.2.1.6.5.2#10, 4.2.1.6.5.2#12)
- ~~32-33.~~ Verify that the PUT transitions to CL0 state

#### TD 4.013 Gen 2/3 CL1 Test (Re-timers on the Link)

*Note: This test is only performed with an Active Cable that contains re-timers. The Active Cable must support CLx states. The test is performed simultaneously for both the Lane 0 Adapter and the Lane 1 Adapter of the Port being tested.*

*Note: This test does not apply at Gen 4 speed. It is performed at Gen 3 speed if supported by the UUT. Otherwise the test is performed at Gen 2 speed.*

- A. Purpose:
  - Verify that the PUT enters CL1 state correctly when there are Re-timers on the Link
  - Verify that the PUT exits CL1 state correctly when there are Re-timers on the Link
- B. Asserts:
  - 4.2.1.3.1#3
  - 4.2.1.6.1#4, 4.2.1.6.1#6
  - 4.2.1.6.1.2#9, 4.2.1.6.1.2#10
  - 4.2.1.6.2#7, 4.2.1.6.2#11, 4.2.1.6.2#13, 4.2.1.6.2#14
  - 4.2.1.6.3#16
  - 4.2.1.6.4#2
  - 4.2.1.6.5.3#9-45, 4.2.1.6.5#48
  - 4.2.4.2#2rt
  - 4.2.4.3.2.1#1rt, 4.2.4.3.2.1#4rt, 4.2.4.3.2.1#5rt
  - 4.2.4.3.2.3#4rt
  - 4.2.4.3.3#2r
- C. Test Setups
  - EX\_HOST\_DFP1 (Host)
  - EX\_DEV\_UFP1 (Device)
  - EX\_HUB\_UFP1 (Hub UFP)
  - EX\_HUB\_DFP1 (Hub DFP)
- D. Repetitions:
  - Repeat with:
    - Exerciser sends CL1\_REQ after the PM Secondary bit is configured
    - Exerciser sends CL1\_REQ after receiving the first CL1\_REQ from the UUT
    - Exerciser does not send CL1\_REQ
  - Repeat with:
    - EXIT\_TIME = tEnterLFPS1
    - EXIT\_TIME = 30 seconds
- E. Background Check:
  - Gen 2/Gen 3 Gen 2/Gen 3 Lane 0/Lane 1 Background Check
- F. Procedure:

USB4 CV performs the following steps:

##### Part 0 – Setup

1. Reset UUT
2. Enumerate UUT Router
3. Initiate Lane Bonding
4. Read the *CL1 Support* bit in the PUT
5. Verify that the *CL1 Support* bit matches the capabilities indicated in the VIF
6. Do not enable Bi-Directional Time Sync Handshakes
7. Configure the PM Secondary
  - a. If the PUT is the UFP, set the *PM Secondary* bit to 1b in the PUT and to 0b in the Exerciser

- b. If the PUT is a DFP, set the *PM Secondary* bit to 0b in the PUT and to 1b in the Exerciser
- 8. Enable CLx states in the PUT and in the Exerciser:
  - a. *CL2 Enable* = 0b
  - b. *CL1 Enable* = 1b
  - c. *CL0s Enable* = 1b
- 9. If both the PUT and Exerciser send CL1\_REQ Ordered Sets at the same time:
  - a. If PUT is not the PM Secondary, perform Part 1
  - b. Else, perform Part 2
- 10. If the Exerciser sends CL1\_REQ Ordered Sets before the PUT:
  - a. If PUT does not support CL1:
    - i. Verify that the PUT sends CL\_NACK Ordered Sets (4.2.1.6.3#16)
    - ii. Perform Part 1
  - b. If PUT sends CL\_NACK Ordered Sets, perform Part 1
  - c. If PUT sends CL1\_ACK Ordered Sets, perform Part 2
- 11. If the PUT sends CL1\_REQ before the Exerciser:
  - a. If Exerciser sends CL\_NACK Ordered Sets, perform Part 3
  - b. If Exerciser sends CL1\_ACK Ordered Sets, perform Part 4
- 12. If neither send CL1\_REQ Ordered Sets, retry test (stop after 5 attempts)

#### Part 1 – PUT Sends CL\_NACK

- 13. If the PUT sent CL1\_REQ Ordered Sets and the PM Secondary bit in the PUT is 0b, verify that the PUT continues to send CL\_NACK Ordered Sets until last CL1\_REQ Ordered Set is sent (4.2.1.6.2#7)
- 14. Else, verify that:
  - a. The PUT sends 16 CL\_NACK Ordered Sets (4.2.1.6.2#13)
  - b. The first CL\_NACK Ordered Set is sent no longer than (tCL0sEntry + tCL0sExit) time after the PUT receives the last CL1\_REQ (4.2.1.6.2#13)
- 15. Parse each CL\_NACK Ordered Set and verify that bits 9:0 (SCR) in the payload are 00 1111 0010b (4.2.1.6.1#6)
- 16. Verify that the PUT is in CL0 state (4.2.1.6.2#14)

#### Part 2 – PUT Sends CL1\_ACK

- 17. Verify that the PUT sends CL1\_ACK Ordered Sets 375 times (4.2.1.6.2#11)

*Note: It is not a failure if the PUT sends more than 375 CL1\_ACK Ordered Sets*

- 18. Parse each CL1\_ACK Ordered Set and verify that bits 9:0 (SCR) in the payload are 00 1111 0010b (4.2.1.6.1#4)
- 19. Perform Part 5

#### Part 3 – Exerciser Sends CL\_NACK

- 20. Verify that the PUT sends back-to-back CL1\_REQ Ordered Sets until it receives CL\_NACK Ordered Sets (4.2.1.6.2#1)
- 20-21. Exerciser continues to send CL\_NACK as long as it receives CL1\_REQ Ordered Sets, after CL2\_REQ are not detected it will move to next step.
- 21-22. Verify that the PUT does not send another CL2\_REQ Ordered Set or CL1\_REQ Ordered Set for at least tCLxRetry (4.2.1.6.2#20)
- 22-23. Verify that the PUT Adapters are in CL0 state (4.2.1.6.2#21)

#### Part 4 – Exerciser Sends CL1\_ACK

- ~~23~~24. Verify that the PUT sent back-to-back CL1\_REQ Ordered Sets until it received CL1\_ACK Ordered Set (4.2.1.6.2#1)
- ~~24~~25. Verify that the PUT sends 375 CL\_OFF Ordered Sets (4.2.1.6.2#17)
- ~~25~~26. Verify that the first CL\_OFF Ordered Set is sent within tCLxResponse after getting the CL1\_ACK (4.2.1.6.2#18)
- ~~26~~27. Verify that the PUT Adapters are in the CL1 state (4.2.1.6.2#26)
- ~~27~~28. Perform Part 5

#### Part 5 – CL1 Exit

- ~~28~~29. Wait EXIT\_TIME time after detecting that the PUT transitioned to CL1 state (see repetitions)
- ~~29~~30. Tell the Exerciser to initiate exit from CL1 state by sending LFPS
- ~~30~~31. Verify that the PUT does the following:
  - a. Sends an LFPS burst on the Lane for at least 5 LFPS cycles (4.2.1.6.5.3#9)
    - i. If PUT contains On-Board Re-timers, LFPS is sent for at least 5 LFPS cycles (4.2.4.3.2.1#1rt)
  - b. Does not send the LFPS burst for more than tLFPSDuration (4.2.1.6.5.3#9)
  - c. Sends the first LFPS within tWarmUpCL1 after receiving the first LFPS cycle (4.2.1.6.5.3#9)
  - d. If PUT does not contain On-Board Re-timers, it starts transmitting SLOS on the Lane (4.2.1.6.5.3#11)
  - e. If PUT contains On-Board Re-timers, it starts transmitting CL\_WAKE1.X Ordered Set Symbols (4.2.4.3.2.1#5rt)
  - f. Upon reception of 3 consecutive and identical CL\_WAKE1.X Ordered Sets, starts transmitting CL\_WAKE2.X Ordered Sets on the Lane (4.2.1.6.5#48, 4.2.1.6.5.3#13)
  - g. CL\_WAKE2.X from PUT are not scrambled (4.2.1.6.1.2#9)
  - h. PUT does not send any partial CL\_WAKE2.X (4.2.1.6.1.2#10)
  - i. If the PUT receives 7 back-to-back CL\_WAKE2.X Ordered Sets, it transitions to Training.LOCK1 substate (4.2.1.3.1#3, 4.2.1.6.5.3#14)
  - j. If the PUT receives 7 back-to-back SLOS Symbols, it transitions to Training.LOCK1 substate (4.2.1.3.1#3, 4.2.1.6.5.3#14)
  - k. If PUT contains On-Board Re-timers, verify that it stops sending CL\_WAKE1.X Ordered Set Symbols (4.2.4.3.2.3#4rt)
- ~~31~~32. Verify that the PUT transitions to CL0 state



#### TD 4.014 Gen 2/3 CL0s Test (No Re-timers on the Link)

*Note: This test only applies to Ports that do not contain any On-Board Re-timers.*

*Note: This test is performed with a Passive Cable to avoid introducing re-timers on the Link. The test is performed simultaneously for both the Lane 0 Adapter and the Lane 1 Adapter of the Port being tested.*

*Note: This test is not performed if the Router does not support CL0s state.*

*Note: This test is only performed on the DFP*

*Note: This test does not apply at Gen 4 speed. It is performed at Gen 3 speed if supported by the UUT. Otherwise the test is performed at Gen 2 speed.*

- A. Purpose:
  - Verify that the PUT Adapters enter CL0s state correctly when there are no Re-timers on the Link
  - Verify that the PUT Adapters exit CL0s state correctly when there are no Re-timers on the Link
- B. Asserts:
  - 4.2.1.4.1#3
  - 4.2.1.6.1#5
  - 4.2.1.6.2#12, 4.2.1.6.2#30
  - 4.2.1.6.4#3
  - 4.2.1.6.5.1#11, 4.2.1.6.5.1#12, 4.2.1.6.5.1#15, 4.2.1.6.5.1#16
- C. Test Setups
  - EX\_HOST\_DFP1 (Host)
  - EX\_HUB\_DFP1 (Hub)
- D. Repetitions:
  - Repeat with:
    - EXIT\_TIME = (375 Symbol Times + 100ns)
    - EXIT\_TIME = 30 seconds
- E. Background Check:
  - Gen 2/Gen 3 Gen 2/Gen 3 Lane 0/Lane 1 Background Check
- F. Procedure:

USB4 CV performs the following steps:

##### Part 0 – Setup

1. Reset UUT
2. Enumerate UUT Router
3. Initiate Lane Bonding
4. Read the *CL0s Support* bit in PUT
5. Verify that the *CL0s Support* bit matches the capabilities indicated in the VIF
6. Enable CLx states in the PUT and the Exerciser:
  - a. *CL2 Enable* = 1b
  - b. *CL1 Enable* = 1b
  - c. *CL0s Enable* = 1b

7. Configure/enable unidirectional timestamps (HiFi mode) for objection to CL2/CL1 in the PUT

Part 1 – Initiate CL0s Entry

8. Tell the Exerciser to send CL2\_REQ Ordered Sets
9. If the PUT does not respond with CL0s\_ACK Ordered Sets, end test here

*Note: it is not a test failure if the PUT does not respond with CL0s\_ACK Ordered Sets*

10. Parse each CL0s\_ACK Ordered Set and verify that bits 9:0 (SCR) in the payload are 00 1111 0010 (4.2.1.6.1#5)
11. Verify that the PUT sends CL0s\_ACK Ordered Sets for 16 symbol times (4.2.1.6.2#12)
12. Send CL\_OFF Ordered Sets to the PUT for 375 symbol times

Part 2 – Initiate CL0s Exit

13. Tell the Exerciser to initiate exit from CL0s state by sending LFPS
14. Verify that the PUT does the following after detecting LFPS:
  - a. On detection of 3 consecutive SLOS Symbols, transmits 10-40 TS2 Ordered Sets (4.2.1.6.5.1#15)
  - b. On detection of 2 consecutive TS2 Ordered Sets, transitions to CL0 state (4.2.1.6.5.1#16, 4.2.1.4.1#3)

#### TD 4.015 Gen 2/3 CL0s Test (Re-timers on the Link)

*Note: This test is only performed with an Active Cable that contains re-timers. The Active Cable must support CLx states. The test is performed simultaneously for both the Lane 0 Adapter and the Lane 1 Adapter of the Port being tested.*

*Note: This test is not performed if the Router does not support CL0s state.*

*Note: This test does not apply at Gen 4 speed. It is performed at Gen 3 speed if supported by the UUT. Otherwise the test is performed at Gen 2 speed.*

A. Purpose:

- Verify that the PUT Adapters enter CL0s state correctly when there are Re-timers on the Link
- Verify that the PUT Adapters exit CL0s state correctly when there are Re-timers on the Link

B. Asserts:

- 4.2.1.4.1#3
- 4.2.1.6.1#5
- 4.2.1.6.2#12, 4.2.1.6.2#30
- 4.2.1.6.4#3
- 4.2.1.6.5.1#11, 4.2.1.6.5.1#12, 4.2.1.6.5.1#15, 4.2.1.6.5.1#16
- 4.2.4.2#3rt
- 4.2.4.3.1#3rt, 4.2.4.3.1#4rt, 4.2.4.3.1#7rt
- 4.2.4.3.3#2rt

C. Test Setups

- EX\_HOST\_DFP1 (Host)
- EX\_DEV\_UFP1 (Device)
- EX\_HUB\_UFP1 (Hub UFP)
- EX\_HUB\_DFP1 (Hub DFP)

D. Repetitions:

- Repeat with:
  - EXIT\_TIME = (375 Symbol Times + 100ns)
  - EXIT\_TIME = 30 seconds

E. Background Check:

- Gen 2/Gen 3 Gen 2/Gen 3 Lane 0/Lane 1 Background Check

F. Procedure:

USB4 CV performs the following steps:

Part 0 - Setup

1. Reset UUT
2. Enumerate UUT Router
3. Initiate Lane Bonding
4. Read the *CL0s Support* bit in PUT
5. Verify that the *CL0s Support* bit matches the capabilities indicated in the VIF
6. Enable CLx states in the PUT and the Exerciser:
  - a. *CL2 Enable* = 1b
  - b. *CL1 Enable* = 1b
  - c. *CL0s Enable* = 1b

7. Configure/enable unidirectional timestamps (HiFi mode) for objection to CL2/CL1 in the PUT

#### Part 1 – Initiate CL0s Entry

8. Tell the Exerciser to send CL2\_REQ Ordered Sets
9. Verify that the PUT responds with CL0s\_ACK Ordered Sets (4.2.1.6.2#12)
10. Parse each CL0s\_ACK Ordered Set and verify that bits 9:0 (SCR) in the payload are 00 1111 0010 (4.2.1.6.1#5)
11. Verify that the PUT sends CL0s\_ACK Ordered Sets for 16 symbol times (4.2.1.6.2#12)
12. Send CL\_OFF Ordered Sets to PUT for 375 symbol times
13. Wait the equivalent of 375 Symbol Times after the PUT sends the first response Ordered Set

#### Part 2 – Initiate CL0s Exit

15. Tell the Exerciser to initiate exit from CL0s state by sending LFPS
16. Verify that the PUT does the following after detecting LFPS:
  - a. If PUT contains On-Board Re-timers, PUT sends CL\_WAKE1.X Ordered Set Symbols (4.2.4.3.1#4rt)
  - b. On reception of 3 consecutive CL\_WAKE1.X Ordered Sets, transmits at least 8 CL\_WAKE2.X Ordered Sets. (4.2.1.6.5.1#12)
  - c. On detection of 3 consecutive SLOS Symbols, transmits 16 TS2 Ordered Sets (4.2.1.6.5.1#15)
  - d. On detection of 2 consecutive TS2 Ordered Sets, transitions to CL0 state (4.2.1.6.5.1#16, 4.2.1.4.1#3)
  - e. If PUT contains On-Board Re-timers, PUT stop sending CL\_WAKE1.X Ordered Set Symbols (4.2.4.3.1#7rt)
17. If PUT contains On-Board Re-timers, verify that the PUT sends CL\_WAKE1.X Ordered Set Symbols

## TD 4.016 CLx Exit Initiation Test

*Note: This test is not performed if the Router does not support CLx states. The test is performed simultaneously for both the Lane 0 Adapter and the Lane 1 Adapter of the Port being tested.*

- A. Purpose:
  - Verify that the PUT initiates exit from CLx states correctly
- B. Asserts:
  - 4.2.1.6.5#1, 4.2.1.6.5.1#1-4, 4.2.1.6.5.1#8-9, 4.2.1.6.5.2#1, 4.2.1.6.5.2#4-6, 4.2.1.6.5.3#1-5
- C. Test Setups
  - EX\_HOST\_DFP1 (Host)
  - EX\_DEV\_UFP1 (Device)
  - EX\_HUB\_UFP1 (Hub UFP) EX\_HUB\_DFP1 (Hub DFP)
- D. Repetitions:
  - Repeat for all supported CLx states
  - [CLx Entry by PUT/Exerciser](#)
- G. Background Check:
  - Gen 2/Gen 3 Lane 0/Lane 1 Background Check
- E. Procedure:

USB4 CV performs the following steps:

### Part 0 - Setup

1. Reset UUT
2. Enumerate UUT Router
3. Initiate Lane Bonding
4. Transition the PUT Adapters to CLx state (see repetitions)
5. If testing CL0s exit, perform Part 1
6. If testing CL1 or CL2 exit and there are no Re-timers on the Link, perform Part 2
7. If testing CL1 or CL2 exit and there are one or more Re-timers in the Link, perform Part 3

### Part 1 – CL0s exit

8. Send the PUT a Read Request to cause the PUT Adapters to exit the CL0s state
9. Verify that the PUT transitions out of CL0s state as follows: (4.2.1.6.5#1)
  - a. PUT sends an LFPS burst on all Lanes for the duration of at least 16 LFPS cycles (4.2.1.6.5.1#1)
  - b. PUT starts transmitting SLOS1 ([or CL\\_WAKE1.X if there is an On-board Re-timer](#)) on each Lane of the USB4 Port (4.2.1.6.5.1#3)
  - c. On detection of 2 back-to-back TS2 Ordered Sets, PUT stops sending SLOS1/[CL\\_WAKE1.X](#) and sends at least 16 TS2 Ordered Sets (4.2.1.6.5.1#4)
  - d. PUT Adapters transition to CL0 state (4.2.1.6.5.1#8)
10. Verify that PUT resumes operation as a Dual-Lane Link (4.2.1.6.5.1#9)
11. Verify that PUT sends a de-skew Ordered Set (4.2.1.6.5.1#9)

### Part 2 – CL1/CL2 Exit (no Re-timers)

9. Send the PUT a Read Request to cause the PUT Adapters to exit the CL1/CL2 state

10. Verify that the PUT transitions out of CL1/CL2 state as follows:
  - a. PUT sends a Low Frequency Periodic Signaling (LFPS) burst on each Lane until the receiver detects LFPS (4.2.1.6.5.2#1)
  - b. PUT starts transmitting SLOS (4.2.1.6.5.2#4)
  - c. PUT Adapters transition to Training.LOCK2 sub-state (4.2.1.6.5.2#6)

Part 3 – CL1/CL2 Exit (On-Board Re-timers)

9. Send the PUT a Read Request to cause the PUT Adapters to exit the CL1/CL2 state
10. Verify that the PUT transitions out of CL1/CL2 state as follows:
  - a. PUT sends a Low Frequency Periodic Signaling (LFPS) burst on each Lane until its receiver detects LFPS (4.2.1.6.5.3#1)
  - b. PUT starts transmitting CL\_WAKE1.X (4.2.1.6.5.3#4)
  - c. Upon reception of 3 back-to-back CL\_WAKE1.X Ordered Set Symbols, PUT starts transmitting CL\_WAKE2.X Ordered Set Symbols (4.2.1.6.5.3#6)
  - d. Upon reception of 7 back-to-back CL\_WAKE2.X Ordered Set Symbols or 7 back-to-back SLOS Symbols, PUT Adapters transition to Training.LOCK1 sub-state (4.2.1.6.5.3#7)

#### TD 4.027 Invalid CLSE Test

A. Purpose:

- Verify that the PUT checks CLSE symbols
- Verify that the PUT drops a Transaction with an invalid CLSE

B. Asserts:

- 4.1.1.2.1#5, 4.1.1.2.1#6

C. Test Setups

- EX\_HOST\_DFP1 (Host)
- EX\_DEV\_UFP1 (Device)
- EX\_HUB\_UFP1 (Hub UFP)
- EX\_HUB\_DFP1 (Hub DFP)

D. Background Check:

- Sideband Channel Background Check

E. Procedure:

*Note: When performing this test on an UFP, the exerciser performs both the test steps that are defined “Upstream of the UUT” and the test steps that are defined “On the PUT”. When this test is performed on a DFP, USB4 CV performs the tests steps that are defined “Upstream of the UUT” and the Exerciser performs the test steps that are defined “On the PUT”.*

Upstream of the UUT:

Part 0 – Setup

1. Reset UUT
2. Enumerate UUT Router
3. Initiate Lane Bonding
4. Wait for Lane Bonding to complete

On the PUT:

Part 1 – Lane 1 Adapter

5. Send an LT\_Fall Transaction to the PUT
  - a. Transaction targets the Lane 1 Adapter
  - b. Transaction has an invalid CLSE
6. Verify that the Lane 1 Adapter is in CL0 state (4.1.1.2.1#5, 4.1.1.2.1#6)

On the PUT:

Part 2 – Lane 0 Adapter

7. Send an LT\_Fall Transaction to the PUT
  - a. Transaction targets the Lane 0 Adapter
  - b. Transaction has an invalid CLSE
8. Verify that the Lane 0 Adapter is in the CL0 state (4.1.1.2.1#5, 4.1.1.2.1#6)

## TD 4.028 Multiple DLE Test

### A. Purpose:

- Verify that the PUT correctly handles AT and RT Transactions with multiple preceding DLE symbols

### B. Asserts:

- 4.1.1.2.4#2

### C. Test Setups

- EX\_HOST\_DFP1 (Host)
- EX\_DEV\_UFP1 (Device)
- EX\_HUB\_UFP1 (Hub UFP)
- EX\_HUB\_DFP1 (Hub DFP)

### D. Repetitions:

- Repeat with AT Transactions
- Repeat with Addressed RT Transactions with the following:
  - *Index* = 0
  - *Index* = First On-Board Re-timer (if present)
  - *Index* = Second On-Board Re-timer (if present)
- Repeat both Transaction types with 2 DLE symbols and 10 DLE symbols

### E. Background Check:

- Sideband Channel Background Check

### F. Procedure:

*Note: When performing this test on an UFP, the exerciser performs both the test steps that are defined “Upstream of the UUT” and the test steps that are defined “On the PUT”. When this test is performed on a DFP, USB4 CV performs the tests steps that are defined “Upstream of the UUT” and the Exerciser performs the test steps that are defined “On the PUT”.*

#### Upstream of the UUT:

1. Reset UUT
2. Enumerate UUT Router
3. Initiate Lane Bonding

#### On the PUT:

4. Send the DLE symbols to the PUT (see repetitions)
5. Immediately after sending the DLE symbols, send the PUT a Write Command with the following:
  - a. *Target* = Register 9 (Metadata)
  - b. *Length* = 4
  - c. *Command Data* = FFFF FFFFh
6. Wait for a Write Response from the PUT
7. Send the PUT a Read Command with the following:
  - a. *Target* = Register 9 (Metadata)
  - b. *Length* = 4
8. Verify that the contents of Register 9 are FFFF FFFFh (4.1.1.2.4#2)



#### TD 4.029 Transaction Error Test

##### A. Purpose:

- Verify that the PUT ignores AT Transactions and Addressed RT Transactions that don't have data and CRC fields.
- Verify that the PUT ignores symbols that are not part of a Transaction
- Verify that the PUT ignores AT Transactions and Addressed RT Transactions with an invalid CRC

##### B. Asserts:

- 4.1.1.2.6#1-4

##### C. Test Setups

- EX\_HOST\_DFP1 (Host)
- EX\_DEV\_UFP1 (Device)
- EX\_HUB\_UFP1 (Hub UFP)
- EX\_HUB\_DFP1 (Hub DFP)

##### D. Repetitions:

- Repeat with AT Transactions
- Repeat with Addressed RT Transactions with the following:
  - Index = 0
  - Index = First On-Board Re-timer (if present)
  - Index = Second On-Board Re-timer (if present)

##### E. Background Check:

- Sideband Channel Background Check

##### F. Procedure:

*Note: When performing this test on an UFP, the exerciser performs both the test steps that are defined "Upstream of the UUT" and the test steps that are defined "On the PUT". When this test is performed on a DFP, USB4 CV performs the tests steps that are defined "Upstream of the UUT" and the Exerciser performs the test steps that are defined "On the PUT".*

#### Upstream of the UUT:

##### Part 0 - Setup

1. Reset UUT
2. Enumerate UUT Router
3. Initiate Lane Bonding

#### On the PUT:

##### Part 1 – Malformed Command

4. Send the PUT a Command with No data symbols and no CRC
5. Verify that the PUT does not send a response (4.1.1.2.6#2)

##### Part 2 – Extra Preceding Symbols

6. Send the PUT a series of 10 extra symbols followed by a Write Command:
  - a. Target = Register 18 (Data)
  - b. COMMAND\_DATA = 12h ... 12h (length 12d)
  - c. Extra symbols are random data (excluding FEh symbol)

7. Verify that the PUT sends a Write Response for the Write Command (4.1.1.2.6#3)
8. Verify that the PUT does not send any other responses (4.1.1.2.6#4)
9. Send the PUT a series of 10 extra symbols followed by a Read Command
  - a. *Target* = Register 18 (Data)
  - b. Extra symbols are random data (excluding FEh symbol)
10. Verify that the PUT sends a Read Response with RESPONSE\_DATA = 12h ... 12h (4.1.1.2.6#3)
11. Verify that the PUT does not send any other responses (4.1.1.2.6#4)

#### Part 3 – Bad CRC

12. Send the PUT a Write Command
  - a. *Target* = Register 18 (Data)
  - b. CRC is invalid
  - d. COMMAND\_DATA = 00 ... 00h (length 12d)
13. Verify that the PUT does not send a Write Response (4.1.1.2.6#1)
14. Send the PUT a Read Command
  - a. *Target* = Register 18 (Data)
  - b. CRC is valid
15. Wait for the PUT to send a Read Response
16. Verify that the value of the RESPONSE\_DATA in the Read Response is the same as what was written in Part 2 (12h ... 12h, length 12d) (4.1.1.2.6#1)

#### Part 3 – Unknown Transaction Type

17. Send the PUT a Transaction that looks like an LT Transaction but contains the following:
  - a. *LSE Symbol* = 0011b (LT\_LRoff)
  - b. Bits [7:6] = 11b (unknown Transaction Type)
18. Verify that the PUT Adapters stay in CL0 state (4.1.1.2.6#3)

#### TD 4.030 SB Register Read Error Test

A. Purpose:

- Verify that the PUT correctly handles Read Request error cases

B. Asserts:

- 4.1.1.3.1#6-10

C. Test Setups

- EX\_HOST\_DFP1 (Host)
- EX\_DEV\_UFP1 (Device)
- EX\_HUB\_UFP1 (Hub UFP)
- EX\_HUB\_DFP1 (Hub DFP)

D. Repetitions:

- Repeat with AT Transactions
- Repeat with Addressed RT Transactions with the following:
  - *Index* = 0
  - *Index* = First On-Board Re-timer (if present)
  - *Index* = Second On-Board Re-timer (if present)

E. Background Check:

- Sideband Channel Background Check

F. Procedure:

*Note: When performing this test on an UFP, the exerciser performs both the test steps that are defined “Upstream of the UUT” and the test steps that are defined “On the PUT”. When this test is performed on a DFP, USB4 CV performs the tests steps that are defined “Upstream of the UUT” and the Exerciser performs the test steps that are defined “On the PUT”.*

#### Upstream of the UUT:

##### Part 0 - Setup

1. Reset UUT
2. Enumerate UUT Router
3. Initiate Lane Bonding

#### On the PUT:

##### Part 1 – Malformed Command (Too Short)

4. Send the PUT a Single Data Symbol
5. Verify that the PUT responds with a Read Response with:
  - a. No RESPONSE\_DATA (4.1.1.3.1#6)
  - b. LEN = 0 (4.1.1.3.1#6)

##### Part 2 – Invalid Target

6. Send the PUT a Read Command that targets an undefined register
7. Verify that the PUT responds with a Read Response with:
  - a. No RESPONSE\_DATA (4.1.1.3.1#7)
  - b. LEN = 0 (4.1.1.3.1#7)

### Part 3 – Malformed Command (Too Long)

8. Send the PUT a Read Command:
  - a. `COMMAND_DATA` = FFh
  - b. `LEN` = 3
9. Verify that the PUT responds with a Read Response with:
  - a. No `RESPONSE_DATA` (4.1.1.3.1#8)
  - b. `LEN` = 0 (4.1.1.3.1#8)

### Part 4 – Long Read (Read > Register Length)

10. Send the PUT a Read Command:
  - a. *Target* = register 1 (Device ID)
  - b. `LEN` = 4
11. Record the `RESPONSE_DATA` returned in the Read Response
12. Send the PUT a Read Command:
  - a. *Target* = Register 1
  - b. `LEN` = 5
13. Verify that the PUT responds with a Read Response with:
  - a. `RESPONSE_DATA` = same as recorded in Step 11 (4.1.1.3.1#9)
  - b. `LEN` = 4 (4.1.1.3.1#9)

### Part 5 – Short Read (Read < Register Length)

14. Send the PUT a Read Command:
  - a. *Target* = Register 1 (Device ID)
  - b. `LEN` = 4
15. Record the `RESPONSE_DATA` returned in the Read Response
16. Send the PUT a Read Command:
  - a. *Target* = Register 1 (Device ID)
  - b. `LEN` = 3
17. Verify that the PUT sends a Read Response with:
  - a. `RESPONSE_DATA` = the first 3 bytes of Register 1 as recorded in Step 15 (4.1.1.3.1#10)
  - b. `LEN` = 4 (4.1.1.3.1#10)

#### TD 4.031 Phase 4 Exit Test

*Note: This test is performed simultaneously for both the Lane 0 Adapter and the Lane 1 Adapter of the Port being tested.*

- A. Purpose:
  - Verify that the PUT Transitions out of Phase 4 correctly under all conditions
- B. Asserts:
  - 4.1.2.4#1, 4.1.2.4#2
- C. Test Setups
  - EX\_HOST\_DFP1 (Host)
  - EX\_DEV\_UFP1 (Device)
  - EX\_HUB\_UFP1 (Hub UFP)
  - EX\_HUB\_DFP1 (Hub DFP)
- D. Background Check:
  - Sideband Channel Background Check
- E. Procedure:

The Exerciser performs the following steps:

##### Part 0 – Setup

1. Drive SBTX to logic low (which will restart Lane Initialization)
2. Perform Lane Initialization through phase 3

##### Part 1 – Broadcast RT Transaction Last

3. Verify that the PUT sends a Broadcast RT Transaction every tLaneParams (4.1.2.4#1)
4. Wait for both to be true:
  - a. At least tLTPhase4 time passed after completing Phase 2
  - b. PUT sent at least 2 Broadcast RT Transactions
5. Send a Broadcast RT Transaction
6. Verify that the PUT stops sending Broadcast RT Transactions (4.1.2.4#2)
7. Finish Lane Initialization

##### Part 2 - Broadcast RT Transaction First

8. Drive SBTX to logic low (which will restart Lane Initialization)
9. Perform Lane initialization through phase 3
10. After receiving two Broadcast RT Transactions, send a Broadcast RT Transaction
11. Verify that the PUT continues to send a Broadcast RT Transaction every tLaneParams until the following are true: (4.1.2.4#2)
  - a. PUT sent at least 2 Broadcast RT Transactions
  - b. At least tLTPhase4 time has passed
12. Verify that the PUT stops sending Broadcast RT Transactions (4.1.2.4#2)
13. Finish Lane Initialization

## TD 4.032 Gen 2/3 Training Delay Test

*Note: This test is performed simultaneously for both the Lane 0 Adapter and the Lane 1 Adapter of the Port being tested.*

*Note: This test does not apply at Gen 4 speed. It is performed at Gen 3 speed if supported by the UUT. Otherwise the test is performed at Gen 2 speed.*

- A. Purpose:
  - Verify that the PUT handles a Link Training delay correctly
- B. Asserts:
  - 4.2.1.3.2#1
  - 4.2.1.4.3#6
- C. Test Setups
  - EX\_HOST\_DFP1 (Host)
  - EX\_DEV\_UFP1 (Device)
  - EX\_HUB\_UFP1 (Hub UFP)
  - EX\_HUB\_DFP1 (Hub DFP)
- D. Background Check:
  - Lane 0/Lane 1 Background Check
- E. Procedure:

The Exerciser performs the following steps:

### Part 1 – TS1 delay

1. Drive SBTX to logic low (which will restart Lane Initialization)
2. Start Lane Initialization
3. After receiving the first SLOS1, CL\_WAKE1.X or SLOS2 from the PUT, start a timer that counts up from 0 in increments of 1ms
4. When the PUT starts sending TS1 OS, continue sending SLOS2 until the timer reaches 900ms (tTrainingAbort1 - tTrainingAbort2)
5. Resume Lane Initialization (send TS1 OS)
6. Verify that PUT transitions to Training.TS2 state (starts sending TS2 OS) (4.2.1.3.2#1)

### Part 2 – TS2 delay

7. Reset UUT
8. Start Lane Initialization
9. After receiving the first SLOS1, CL\_WAKE1.X or SLOS2 from the PUT, start a timer that counts up from 0 in increments of 1ms. When the PUT starts sending TS2 OS, continue sending TS1 OS until the timer reaches 900ms (tTrainingAbort1 - tTrainingAbort2)
10. Resume Lane Initialization (send TS2 OS to PUT)
11. Verify that the PUT transitions to CL0 state (4.2.1.3.2#1)
12. Finish Lane Initialization

### Part 3 – TS1→Lock2

13. Reset UUT
14. Start Lane Initialization
15. Continue sending SLOS2 until PUT starts sending TS1 OS
16. Send PUT one TS1 OS, then send SLOS1

*Note: When RS-FEC is on, the first  $n$  SLOS symbols will be RS-FEC encoded (at Gen 2 speed,  $32 \leq n \leq 64$ ; at Gen 3 speed,  $16 \leq n \leq 32$ ). After sending  $n$  SLOS symbols, RS-FEC is turned off.*

17. Verify that the PUT sends SLOS (4.2.1.3.2#1, 4.2.1.4.3#6)
18. Finish Lane Initialization

#### Part 4 – TS2→Lock2

19. Reset UUT
20. Start Lane Initialization
21. Continue sending TS1 OS until PUT starts sending TS2 OS
22. Send PUT one TS2 OS, then send SLOS1

*Note: When RS-FEC is on, the first  $n$  SLOS symbols will be RS-FEC encoded (at Gen 2 speed,  $32 \leq n \leq 64$ ; at Gen 3 speed,  $16 \leq n \leq 32$ ). After sending  $n$  SLOS symbols, RS-FEC is turned off.*

23. Verify that the PUT sends SLOS (4.2.1.3.2#1, 4.2.1.4.3#6)
24. Finish Lane Initialization

## TD 4.033 Gen 2/3 Training Fail Test

*Note: This test is performed simultaneously for both the Lane 0 Adapter and the Lane 1 Adapter of the Port being tested.*

*Note: This test does not apply at Gen 4 speed. It is performed at Gen 3 speed if supported by the UUT. Otherwise the test is performed at Gen 2 speed.*

- A. Purpose:
  - Verify that the PUT handles Link Training failure correctly
- B. Asserts:
  - 4.2.1.3.2#1
  - 4.2.1.3.3#4
  - 4.2.1.4.3#6
  - 4.2.1.2.2#4
- C. Test Setups
  - EX\_HOST\_DFP1 (Host)
  - EX\_DEV\_UFP1 (Device)
  - EX\_HUB\_UFP1 (Hub UFP)
  - EX\_HUB\_DFP1 (Hub DFP)
- D. Background Check:
  - Lane 0/Lane 1 Background Check
- E. Procedure:

The Exerciser performs the following steps:

### Part 1 – Lock Failure

1. Drive SBTX to logic low (which will restart Lane Initialization)
2. Perform Lane Initialization
3. Mark the time when the PUT starts sending SLOS or CL\_WAKE1.X (i.e. first enters Training state)
4. When PUT starts sending TS1 OS, continue sending SLOS2
5. Verify that the PUT sends TS1 OS for tTrainingAbort1 time after entering Training State (4.2.1.3.2#1)
6. Verify that the PUT starts Lane Initialization from Phase 1 after sending the last TS1 OS (SBTX goes to logic low) (4.2.1.2.2#4)

### Part 2 – TS2 Failure

7. Mark the time when the PUT starts sending SLOS or CL\_WAKE1.X (i.e. first enters Training state)
8. When PUT starts sending TS2 OS, continue sending TS1
9. Verify that the PUT sends TS2 OS for tTrainingAbort1 time (4.2.1.3.2#1)
10. Verify that the PUT starts Lane Initialization from Phase 1 after sending the last TS2 OS (SBTX goes to logic low) (4.2.1.2.2#4)

### Part 3 – Failure After CL0

11. Complete Lane Initialization (PUT Adapters are in CL0 state)
12. Start sending SLOS1 Symbols
13. Mark the time when the PUT starts sending SLOS (i.e. first enters Training state)
14. Verify that the PUT Adapters send SLOS1 or SLOS2(4.2.1.4.3#6)



15. Continue sending back-to-back SLOS1/SLOS2 for tTrainingAbort2 time
16. Verify that the PUT sends SLOS1/SLOS2 for tTrainingAbort2 time after entering Training State (4.2.1.3.3#4)
17. Verify that it starts Lane Initialization from Phase 1 after sending the last SLOS1/SLOS2 (SBTX goes to logic low) (4.2.1.2.2#4)

#### TD 4.034 Gen 2/3 Bonding Delay Test

*Note: This test is performed simultaneously for both the Lane 0 Adapter and the Lane 1 Adapter of the Port being tested.*

*Note: This test does not apply at Gen 4 speed. It is performed at Gen 3 speed if supported by the UUT. Otherwise the test is performed at Gen 2 speed.*

- A. Purpose:
  - Verify that the PUT handles delay in Bonding State correctly
- B. Asserts:
  - 4.2.1.5.2#1
- C. Test Setups
  - EX\_HOST\_DFP1 (Host)
  - EX\_DEV\_UFP1 (Device)
  - EX\_HUB\_UFP1 (Hub UFP)
  - EX\_HUB\_DFP1 (Hub DFP)
- D. Background Check:
  - Lane 0/Lane 1 Background Check
- E. Procedure:

*Note: When performing this test on an UFP, the exerciser performs both the test steps that are defined “Upstream of the UUT” and the test steps that are defined “On the PUT”. When this test is performed on a DFP, USB4 CV performs the tests steps that are defined “Upstream of the UUT” and the Exerciser performs the test steps that are defined “On the PUT”.*

Upstream of the UUT:

##### Part 0 – Setup

1. Reset UUT
2. Enumerate UUT Router
3. Initiate Lane Bonding

On the PUT:

##### Part 1 – TS1 delay

4. When PUT starts sending TS2 OS, continue sending TS1 OS for 20 $\mu$ s (tBonding min – 20 $\mu$ s)
5. Resume Lane Bonding (send TS2 OS to PUT)
6. Verify that the PUT starts sending TS2 OS (4.2.1.5.2#1)
7. Finish Lane Initialization

##### Part 2 – TS1→Lock2

8. Drive SBTX to logic low (which will restart Lane Initialization)
9. Complete Lane Initialization
10. Initiate Lane Bonding
11. When PUT starts sending TS1 OS, send SLOS1
12. Verify that the PUT sends SLOS (4.2.1.5.2#1)
13. Finish Lane Initialization

Part 3 – TS2→Lock2

14. Drive SBTX to logic low (which will restart Lane Initialization)
15. Start Lane Initialization
16. Initiate Lane Bonding
17. When the PUT starts sending TS1 OS, send TS1 OS but do not send any TS2 OS
18. When the PUT starts sending TS2 OS, send SLOS1
19. Verify that the PUT sends SLOS (4.2.1.5.2#1)
20. Finish Lane Initialization

## TD 4.035 Gen 2/3 Bonding Fail Test

*Note: This test is performed simultaneously for both the Lane 0 Adapter and the Lane 1 Adapter of the Port being tested.*

*Note: This test does not apply at Gen 4 speed. It is performed at Gen 3 speed if supported by the UUT. Otherwise the test is performed at Gen 2 speed.*

- A. Purpose:
  - Verify that the PUT initiates a disconnect when Lane bonding fails
- B. Asserts:
  - 4.2.2.2#6
- C. Test Setups
  - EX\_HOST\_DFP1 (Host)
  - EX\_DEV\_UFP1 (Device)
  - EX\_HUB\_UFP1 (Hub UFP)
  - EX\_HUB\_DFP1 (Hub DFP)
- D. Background Check:
  - Lane 0/Lane 1 Background Check
- E. Procedure:

*Note: When performing this test on an UFP, the exerciser performs both the test steps that are defined “Upstream of the UUT” and the test steps that are defined “On the PUT”. When this test is performed on a DFP, USB4 CV performs the tests steps that are defined “Upstream of the UUT” and the Exerciser performs the test steps that are defined “On the PUT”.*

Upstream of the UUT:

### Part 0 – Setup

1. Reset UUT
2. Enumerate UUT Router
3. Initiate Lane Bonding

On the PUT:

### Part 1 – No TS OS

4. If the PUT is a DFP:
  - a. When PUT sends TS1 OS, exerciser does not send TS1s for at least max tBonding time so that bonding fails.
5. If the PUT is a UFP:
  - a. Exerciser sends TS1s until the PUT sends TS1 OS.
  - b. Exerciser continues sending TS1 OS for at least the max tBonding time so that bonding fails.
6. If PUT restarts lane initialization, and it is not in CL0 after tBonding time, verify that it drives SBTX to logic Low.
7. If the PUT drives SBTX to logic Low:
  - a. Verify that SBTX logic Low does not happen before tBonding time.
  - b. Verify that the PUT drives SBTX to logic Low for at least tDisconnectTx (4.2.2.2#6)
8. Complete Lane Initialization

#### Part 2 – Incorrect TS OS

9. Send 2 to 6 TS1 OS with Lane Bonding Target = 001b to initiate Lane Bonding.
10. Send TS1 OS with Lane Bonding Target = 000b to both Adapters
11. Continue sending TS1 for at least the max tBonding time so that bonding fails
12. If PUT restarts lane initialization, and it is not in CL0 after tBonding time, verify that it drives SBTX to logic Low.
13. If the PUT drives SBTX to logic Low:
  - a. Verify that SBTX logic Low does not happen before tBonding time.
  - b. Verify that the PUT drives SBTX to logic Low for at least tDisconnectTx (4.2.2.2#6)
14. Complete Lane Initialization

#### Part 3 – CL0 timeout

15. Send 2 to 6 TS1 OS with Lane Bonding Target = 001b to initiate Lane Bonding
16. Send TS1 OS with Lane Bonding Target = 00b to the Lane 1 Adapter:
  - a. Send TS1 OS with Lane Bonding Target = 001b to the Lane 0 Adapter
17. Continue sending TS1 OS for at least the max tBonding time so that Bonding fails
18. If PUT ~~restarts lane initialization, and it~~ is not in CL0 after tBonding time, verify that it drives SBTX to logic Low.
19. ~~If~~When the PUT drives SBTX to logic Low:
  - a. Verify that SBTX logic Low does not happen before tBonding time.
  - b. Verify that the PUT drives SBTX to logic Low for at least tDisconnectTx (4.2.2.2#6)

#### TD 4.036 Gen 2/3 TS1 Rsvd Bits Ignored Test

*Note: This test is performed simultaneously for both the Lane 0 Adapter and the Lane 1 Adapter of the Port being tested.*

*Note: This test does not apply at Gen 4 speed. It is performed at Gen 3 speed if supported by the UUT. Otherwise the test is performed at Gen 2 speed.*

- A. Purpose:
  - Verify that the PUT ignores reserved bits in TS1 Ordered Sets
- B. Asserts:
  - 4.2.1.3.5#2, 4.2.1.3.5#5, 4.2.1.3.5#7, 4.2.1.3.5#9-10
- C. Test Setups
  - EX\_HOST\_DFP1 (Host)
  - EX\_DEV\_UFP1 (Device)
  - EX\_HUB\_UFP1 (Hub UFP)
  - EX\_HUB\_DFP1 (Hub DFP)
- D. Background Check:
  - Lane 0/Lane 1 Background Check
- E. Procedure:

The Exerciser performs the following steps:

1. Drive SBTX to logic low (which will restart Lane Initialization)
2. Perform Lane Initialization
3. During Training state, send the PUT TS1 Ordered Sets with non-zero values in the following Rsvd fields:
  - a. 63:59
  - b. 47:32
  - c. 31:29
  - d. 28:26
  - e. 25:16

*Note: All TS1 from the Exerciser should have non-zero Rsvd fields.*

4. Verify that the PUT transitions to TS2 state (i.e. stops sending TS1, then sends at least 8 TS2) (4.2.1.3.5#2, 4.2.1.3.5#5, 4.2.1.3.5#7, 4.2.1.3.5#9, 4.2.1.3.5#10)

#### TD 4.037 Gen 2/3 CLx Entry Errors Test

*Note: This test is not performed if the Router does not support CLx states.*

*Note: This test is performed simultaneously for both the Lane 0 Adapter and the Lane 1 Adapter of the Port being tested.*

*Note: This test does not apply at Gen 4 speed. It is performed at Gen 3 speed if supported by the UUT. Otherwise the test is performed at Gen 2 speed.*

- A. Purpose:
  - Verify that the PUT handles errors while entering low power states
- B. Asserts:

- 4.2.1.6.2#38
- C. Test Setups
  - EX\_HOST\_DFP1 (Host)
  - EX\_DEV\_UFP1 (Device)
  - EX\_HUB\_UFP1 (Hub UFP)
  - EX\_HUB\_DFP1 (Hub DFP)
- D. Repetitions:
  - Repeat for all supported CLx states
- E. Background Check:
  - Lane 0/Lane 1 Background Check
- F. Procedure:

*Note: When performing this test on an UFP, the exerciser performs both the test steps that are defined “Upstream of the UUT” and the test steps that are defined “On the PUT”. When this test is performed on a DFP, USB4 CV performs the tests steps that are defined “Upstream of the UUT” and the Exerciser performs the test steps that are defined “On the PUT”.*

Upstream of the UUT:

#### Part 0 - Setup

1. Reset UUT
2. Enumerate UUT Router
3. Initiate Lane Bonding
4. Wait for Lane Bonding to complete
5. If testing CL2 state:
  - a. Set the *CL2 Enable* bit to 1b on both sides of the Link
  - b. Set the *CL1 Enable* bit to 1b on both sides of the Link
  - c. Set the *CL0s Enable* bit to 1b on both sides of the Link
  - d. Do not send any Transport Layer Packets
  - e. Do not configure any Paths (Path 0 should be the only Path)
  - f. Disable Time Sync Handshakes by setting *TSPacketInterval* to 0
6. If testing CL1 state:
  - a. Set the *CL2 Enable* bit to 0b on both sides of the Link
  - b. Set the *CL1 Enable* bit to 1b on both sides of the Link
  - c. Set the *CL0s Enable* bit to 1b on both sides of the Link
  - d. Do not send any Transport Layer Packets
  - e. Do not configure any Paths (Path 0 should be the only Path)
  - f. Disable Time Sync Handshakes by setting *TSPacketInterval* to 0
7. If testing CL0s state:
  - a. Set the *CL2 Enable* bit to 0b on both sides of the Link
  - b. Set the *CL1 Enable* bit to 1b on both sides of the Link
  - c. Set the *CL0s Enable* bit to 1b on both sides of the Link
  - d. Do not send any Transport Layer Packets
  - e. Do not configure any Paths (Path 0 should be the only Path)
  - f. Configure both the PUT and Link Partner to use HiFi Uni-Directional Time Sync Handshakes:
    - i. Write 10h to the *TSPacketInterval* field in Router Configuration Space
    - ii. Write 1b to the *EnableUniDirectionalMode* field in the Lane 0 Adapter Configuration Space
    - iii. Write 0b to the *Disable Time Sync* field in the Lane 0 Adapter Configuration Space.
8. Configure both PUT Adapters with *PM Secondary* = 1b

9. Tell Exerciser to perform the test

On the PUT:

Part 1 – Link Error

10. Initiate entry to CLx state (see repetitions):
  - a. If requesting entry to CL2 state, send the PUT back-to-back CL2\_REQ
  - b. Else, send the PUT back-to-back CL1\_REQ
11. Wait for the PUT to send Response Ordered Set
  - a. If testing CL2, Response Ordered Set = CL2\_ACK
  - b. If testing CL1, Response Ordered Set = CL1\_ACK
  - c. If testing CL0s, Response Ordered Set = CL0s\_ACK

*Note: It is not a test failure if the PUT sends CL\_NACK. If the PUT sends CL\_NACK, retry the test. If after 3 attempts the test cannot be run, print a warning and continue on to the next test.*

12. After receiving the CLx\_ACK response from the PUT, send 2 to 5 unknown Ordered Sets before sending CL\_OFF
13. Continue to send CL\_OFF to complete the target CLx state transition
14. Verify that the PUT does not enter Training state (4.2.1.6.2#38)
15. Verify that the PUT finishes the transition to the target CLx state



#### TD 4.038 Gen 2/3 CL0s Exit Errors Test

*Note: This test is only performed if the Router supports both CL1 state and CL0s state.*

*Note: [This test is not run if Time Synchronization Protocol Not Supported \(TSNS\) is 1.](#) Note: This test is performed simultaneously for both the Lane 0 Adapter and the Lane 1 Adapter of the Port being tested.*

*Note: For Part 1 of this test, the Exerciser emulates two Re-timers on the Link (X=2).*

*Note: This test does not apply at Gen 4 speed. It is performed at Gen 3 speed if supported by the UUT. Otherwise the test is performed at Gen 2 speed.*

- A. Purpose:
  - Verify that the PUT handles errors while exiting CL0s state
- B. Asserts:
  - 4.2.1.6.5.1#13, 4.2.1.6.5.1#17
- C. Test Setups
  - EX\_HOST\_DFP1 (Host)
  - EX\_DEV\_UFP1 (Device)
  - EX\_HUB\_UFP1 (Hub UFP)
  - EX\_HUB\_DFP1 (Hub DFP)
- D. Repetitions:
  - Repeat for all supported CLx states
- E. Background Check:
  - Lane 0/Lane 1 Background Check
- F. Procedure:

*Note: When performing this test on an UFP, the exerciser performs both the test steps that are defined “Upstream of the UUT” and the test steps that are defined “On the PUT”. When this test is performed on a DFP, USB4 CV performs the tests steps that are defined “Upstream of the UUT” and the Exerciser performs the test steps that are defined “On the PUT”.*

Upstream of the UUT:

##### Part 0 – Setup

1. Reset UUT
2. Enumerate UUT Router
3. Initiate Lane Bonding
4. Wait for Lane Bonding to complete
5. Configure both the PUT and Link Partner to use HiFi Uni-Directional Time Sync Handshakes:
  - a. Write 10h to the *TSPacketInterval* field in Router Configuration Space
  - b. Write 1b to the *EnableUniDirectionalMode* field in the Lane 0 Adapter Configuration Space
  - c. Write 0b to the *Disable Time Sync* field in the Lane 0 Adapter Configuration Space.
6. Enable CLx states in both the PUT and Link Partner:
  - a. Set the *CL2 Enable* bit to 1b on both sides of the Link
  - b. Set the *CL1 Enable* bit to 1b on both sides of the Link
  - c. Set the *CL0s Enable* bit to 1b on both sides of the Link

The Exerciser performs the following steps:

Part 0 – Setup

7. Transition PUT Adapters to CL0s state (PUT Rx is off)
  - a. Send the PUT CL1\_REQ
  - b. Wait for PUT to send CL0s\_ACK
  - c. Send CL\_OFF

*Note: It is not a test failure if the PUT sends CL\_NACK. If the PUT sends CL\_NACK, retry the test. If after 3 attempts the test cannot be run, print a warning and continue on to the next test.*

Part 1 – tCL0sSwitch Timeout

8. Initiate exit from CL0s state
  - a. Send LFPS burst on all Lanes for 16 LFPS cycles
  - b. Return to electrical idle for tPreData
  - c. Send back-to-back CL\_WAKE1.X Ordered Set Symbols
  - d. Do not send any additional SLOS or CL\_WAKE.(X+1) symbols
9. Wait tCL0sSwitch time
10. Verify that the PUT Adapters transition to the Training.LOCK1 substate (4.2.1.6.5.1#13)

Part 2 – tTS2Timeout Timeout

11. Transition PUT to CL0s state
12. Initiate exit from CL0s state:
  - a. Send LFPS burst on all Lanes for 16 LFPS cycles
  - b. Return to electrical idle for tPreData
  - c. Send back-to-back SLOS symbols and ignore received TS2 Symbols
13. Wait tTS2Timeout time
14. Verify that the PUT transitions to the Training state (4.2.1.6.5.1#17)

#### TD 4.039 Gen 2/3 RS-FEC Correctable Error Test

*Note: This test does not apply at Gen 4 speed. It is performed at Gen 3 speed if supported by the UUT. Otherwise the test is performed at Gen 2 speed.*

- A. Purpose:
  - Verify that the PUT can correct up to two 1-byte errors in an RS-FEC block
- B. Asserts:
  - 4.3.6#13
- C. Test Setups
  - EX\_HOST\_DFP1 (Host)
  - EX\_DEV\_UFP1 (Device)
  - EX\_HUB\_UFP1 (Hub UFP)
  - EX\_HUB\_DFP1 (Hub DFP)
- D. Repetitions:
- E. Background Check:
  - Lane 0/Lane 1 Background Check
- F. Procedure:

USB4 CV performs the following steps:

1. Reset UUT
2. Tell the Exerciser to generate correctable errors

*Note: The Exerciser injects randomly spaced errors so that either one or two errors fall within an RS-FEC block*

3. Enumerate the UUT Router
4. Verify that the PUT sends a Read Response for each Read Request it receives (4.3.6#13)
5. Initiate Lane Bonding
6. Wait tBonding time
7. Verify that the Lane Adapters on either side of the Link are in CL0 state and the Link is x2. (4.3.6#13)
8. Read bit 5 (RS-FEC Decoder Error) in the *Logical Layer Errors* field
9. Verify that bit 5 (RS-FEC Decoder Error) in the *Logical Layer Errors* field is 0b (4.3.6#13)
10. Verify that the Link does not go down at any time while the Exerciser is generating correctable errors (4.3.6#13)

## TD 4.040 Gen 2/3 Unknown Ordered Set Link Error Test

*Note: This test does not apply at Gen 4 speed. It is performed at Gen 3 speed if supported by the UUT. Otherwise the test is performed at Gen 2 speed.*

### A. Purpose:

- Verify that the PUT detects and reports Link errors correctly

### B. Asserts:

- 4.2.1.3.1#2
- 4.2.1.4.3#5
- 4.2.2.2.1#1
- 4.4.2#1-4, 4.4.2#9-12

### C. Test Setups

- EX\_HOST\_DFP1 (Host)
- EX\_DEV\_UFP1 (Device)
- EX\_HUB\_UFP1 (Hub UFP)
- EX\_HUB\_DFP1 (Hub DFP)

### D. Repetitions:

- Repeat with Adapters in CL0 state and in Training state (4.4.2#4)
- Repeat for Lane 1 Adapter and Lane 0 Adapter

*Note: When testing a Lane 1 Adapter, the Notification Packets may be sent on Lane 0.*

### E. Background Check:

- Lane 0/Lane 1 Background Check

### F. Procedure:

*Note: When performing this test on an UFP, the exerciser performs both the test steps that are defined “Upstream of the UUT” and the test steps that are defined “On the PUT”. When this test is performed on a DFP, USB4 CV performs the tests steps that are defined “Upstream of the UUT” and the Exerciser performs the test steps that are defined “On the PUT”.*

Upstream of the UUT:

#### Part 0 - Setup

1. Disable RS-FEC
  - a. For Gen 2, set the *RS-FEC Request (Gen 2)* bit to 0b in the PUT and Link Partner
  - b. For Gen 3, set the *RS-FEC Request (Gen 3)* bit to 0b in the PUT and Link Partner
2. Reset UUT
3. Enumerate UUT Router
4. Initiate lane bonding
5. Write 1b to each bit in the *Logical Layer Errors Enable* field in Adapter Configuration Space of the Lane 0 Adapter
6. Read the value of the *Logical Layer Errors Enable* field in Adapter Configuration Space of the Lane 0 Adapter:
  - a. If a bit is 1b, then PUT supports that error
  - b. If a bit is 0b, the PUT does not support that error
7. Verify that the PUT supports Ordered Set Errors (4.4.2#1)
8. Verify that each PUT reports the same supported errors (4.4.2#3)

#### Part 1 – Ordered Set Errors (OSE Notification Disabled)

9. Write 0b to each bit in the *Logical Layer Errors Enable* field in Adapter Configuration Space of the Lane 0 Adapter
10. Read the *Logical Layer Errors* field in Adapter Configuration Space of the Lane 0 Adapter to clear any previous errors

#### On the PUT:

11. While PUT Adapters are in the target state (see repetitions), send the PUT 2 back-to-back Ordered Sets with unknown contents
12. Verify that:
  - a. Both Adapters entered Training.LOCK1 sub-state (i.e. sent SLOS1) (4.2.2.2.1#1, 4.2.1.3.1#2, 4.2.1.4.3#5, 4.4.2#9)
  - b. PUT transitioned to CL0 state (i.e. stops sending TS2 OS) within tTrainingAbort2 after sending the first SLOS1 (4.2.1.3.3#3)

#### Upstream of the UUT:

13. Send the PUT a Read Request to read the *Logical Layer Errors* field in Adapter Configuration Space of the Lane 0 Adapter
14. Verify that the PUT:
  - a. Sets the OSE bit in *Logical Layer Errors* field to 1b (4.4.2#10)
  - b. Does not send any Notification Packets with Event Code = ERR\_LINK (4.4.2#12)
15. Set the OSE bit (bit 1) in the *Logical Layer Errors Enable* field to 1b
16. Read the *Logical Layer Errors* field in Adapter Configuration Space of the Lane 0 Adapter to clear the previous error

#### Part 2 – Ordered Set Errors (OSE Notification Enabled)

#### On the PUT:

17. While PUT Adapters are in the target state (see repetitions), send the PUT 2 back-to-back Ordered Sets with unknown contents
18. Verify that:
  - a. The PUT Adapters go to Training.LOCK1 sub-state (i.e. sent SLOS1) (4.2.1.3.1#2, 4.2.1.4.3#5, 4.4.2#9)
  - b. PUT transitioned to CL0 state (i.e. stops sending TS2 OS) within tTrainingAbort2 after sending the first SLOS1 (4.2.1.3.3#3)

#### Upstream of the UUT:

19. Send the PUT a Read Request to read the *Logical Layer Errors* field in Adapter Configuration Space of the Lane 0 Adapter
20. Parse the Read Response from the PUT and verify that the PUT sets the OSE bit (bit 1) in *Logical Layer Errors* field to 1b (4.4.2#10)
21. Verify that the PUT sends a Notification Packet with Event Code = ERR\_LINK and the Adapter Num field set to the Lane that the error occurred on (see repetitions) (4.4.2#11)

#### TD 4.041 Gen 2/3 Uncorrectable SCR Link Error Test

*Note: This test does not apply at Gen 4 speed. It is performed at Gen 3 speed if supported by the UUT. Otherwise the test is performed at Gen 2 speed.*

- A. Purpose:
  - Verify that the PUT detects and reports Link errors correctly
- B. Asserts:
  - 4.2.1.3.1#2
  - 4.2.1.4.3#5
  - 4.2.2.2.1#1
  - 4.4.2#4, 4.4.2#9-12
- C. Test Setups
  - EX\_HOST\_DFP1 (Host)
  - EX\_DEV\_UFP1 (Device)
  - EX\_HUB\_UFP1 (Hub UFP)
  - EX\_HUB\_DFP1 (Hub DFP)
- D. Repetitions:
  - Repeat at Gen 2 and Gen 3 speeds (if supported)
  - Repeat for Lane 1 Adapter and Lane 0 Adapter
- E. Background Check:
  - Lane 0/Lane 1 Background Check
- F. Procedure:

*Note: When performing this test on an UFP, the exerciser performs both the test steps that are defined “Upstream of the UUT” and the test steps that are defined “On the PUT”. When this test is performed on a DFP, USB4 CV performs the tests steps that are defined “Upstream of the UUT” and the Exerciser performs the test steps that are defined “On the PUT”.*

Upstream of the UUT:

##### Part 0 - Setup

1. Disable RS-FEC
  - a. For Gen 2, set the *RS-FEC Request (Gen 2)* bit to 0b in the PUT and Link Partner
  - b. For Gen 3, set the *RS-FEC Request (Gen 3)* bit to 0b in the PUT and Link Partner
2. Reset UUT
3. Enumerate UUT Router
4. Initiate lane bonding

##### Part 1 – Ordered Set Errors – Uncorrectable SCR (OSE Notification Disabled)

5. Configure PUT with the OSE bit in the *Logical Layer Errors Enable* field set to 0b in the Lane 0 Adapter
6. Read the *Logical Layer Errors* field in the Lane 0 Adapter to clear any previous errors

On the PUT:

7. Send the PUT 2 back-to-back Ordered Sets with an uncorrectable error in the SCR field

8. Verify that :
  - a. Both PUT Adapters go to Training.LOCK1 sub-state (i.e. sent SLOS1) (4.2.1.3.1#2, 4.2.1.4.3#5, 4.2.2.2.1#1, 4.4.2#9)
  - b. PUT transitioned to CL0 state (i.e. stops sending TS2 OS) within tTrainingAbort2 after sending the first SLOS1 (4.2.1.3.3#3)

Upstream of the UUT:

9. Send the PUT a Read Request to read the *Logical Layer Errors* field in Adapter Configuration Space of the Lane 0 Adapter
10. Verify that the PUT:
  - a. Sets the OSE bit in *Logical Layer Errors* field to 1b (4.4.2#10)
  - b. Does not send a Notification Packet (4.4.2#12)
11. Configure PUT with the OSE bit in the *Logical Layer Errors Enable* field set to 1b

#### Part 2 – Ordered Set Errors – Uncorrectable SCR (OSE Notification Enabled)

On the PUT:

12. Send the PUT 2 back-to-back Ordered Sets with an uncorrectable error in the SCR field
13. Verify that:
  - a. The PUT Adapters go to Training.LOCK1 sub-state (i.e. sent SLOS1) (4.2.1.3.1#2, 4.2.1.4.3#5, 4.4.2#9)
  - b. PUT transitioned to CL0 state (i.e. stops sending TS2 OS) within tTrainingAbort2 after sending the first SLOS1 (4.2.1.3.3#3)

Upstream of the UUT:

14. Send the PUT a Read Request to read the *Logical Layer Errors* field in Adapter Configuration Space of the Lane 0 Adapter
15. Parse the Read Response from the PUT and verify that the PUT sets the OSE bit in *Logical Layer Errors* field to 1b (4.4.2#10)
16. Verify that the PUT sends a Notification Packet with Event Code = ERR\_LINK (4.4.2#11)

## TD 4.042 Gen 2/3 Timeout Link Error Test

*Note: This test does not apply at Gen 4 speed. It is performed at Gen 3 speed if supported by the UUT. Otherwise the test is performed at Gen 2 speed.*

A. Purpose:

- Verify that the PUT detects and reports Link errors correctly

B. Asserts:

- 4.4.2#4, 4.4.2#15-16

C. Test Setups

- EX\_HOST\_DFP1 (Host)
- EX\_DEV\_UFP1 (Device)
- EX\_HUB\_UFP1 (Hub UFP)
- EX\_HUB\_DFP1 (Hub DFP)

D. Repetitions:

- Repeat for Lane 1 Adapter and Lane 0 Adapter as the Target Adapter

E. Background Check:

- Lane 0/Lane 1 Background Check

F. Procedure:

*Note: When performing this test on an UFP, the exerciser performs both the test steps that are defined “Upstream of the UUT” and the test steps that are defined “On the PUT”. When this test is performed on a DFP, USB4 CV performs the tests steps that are defined “Upstream of the UUT” and the Exerciser performs the test steps that are defined “On the PUT”.*

### Upstream of the UUT:

#### Part 0 - Setup

1. Reset UUT
2. Enumerate UUT Router
3. Write 1b to the TE bit in the *Logical Layer Errors Enable* field in the Adapter Configuration Space of the Target Adapter (see repetitions)
4. Read the value of the *Logical Layer Errors Enable* field in the Adapter Configuration Space of the Target Adapter:
  - a. If the TE bit is 1b (PUT supports TE errors), continue to Part 1
  - b. If the TE bit is 0b (PUT does not support TE errors), end test here

#### Part 1 – Timeout Errors (TE Notification Disabled)

5. Configure the Target Adapter with the TE bit in the *Logical Layer Errors Enable* field set to 0b
6. Read the *Logical Layer Errors* field in the Target Adapter to clear any previous errors

### On the PUT:

7. Transition the Adapters in the PUT to Training state
8. Note when the PUT sends the first SLOS1 (i.e. enters Training state)
9. On the Target Adapter, after entering the Training.TS1 state, only send TS1



10. Continue sending TS1 until at least tTrainingError (500µs) time passes after the first SLOS1 was received from the PUT (this should cause the timeout error to occur)
11. Resume Link training and bring both Adapters to CL0 state

*Note: After the timeout error occurs, an Adapter can either continue Link Training or transition to the Training.LOCK1 state.*

12. Verify that the Adapter did not restart Link Initialization (disconnect) unless the Adapter was in Training state for more than 100ms (tTrainingAbort2)

Upstream of the UUT:

13. Wait for the PUT Adapters to reach CL0 state
14. Send the Target Adapter a Read Request to read the *Logical Layer Errors* field in Adapter Configuration Space
15. Verify that the Target Adapter:
  - a. Sets the TE bit in the *Logical Layer Errors* field to 1b (4.4.2#14)
  - b. Does not send a Notification Packet (4.4.2#16)
16. Configure the Target Adapter with the TE bit in the *Logical Layer Errors Enable* field set to 1b

#### Part 2 – Timeout Errors (TE Notification Enabled)

On the PUT:

17. Transition the Adapters in the PUT to Training state
18. On the Target Adapter, only send TS1 (to prevent transition to CL0 state)
19. Wait at least tTrainingError (500µs) for timeout error to occur
20. When the PUT Adapters enter the Training.LOCK1 state (i.e. sends SLOS1) , continue with Link training and bring both Adapters to CL0 state

Upstream of the UUT:

21. Wait for the PUT Adapters to reach CL0 state
22. Send the Target Adapter a Read Request to read the *Logical Layer Errors* field in Adapter Configuration Space
23. Parse the Read Response from the Target Adapter and verify that the Target Adapter sets the TE bit in the *Logical Layer Errors* field to 1b (4.4.2#14)
24. Verify that the PUT sends a Notification Packet with Event Code = ERR\_LINK (4.4.2#15)

#### TD 4.043 Gen 2/3 Rx De-Skew Test

*Note: This test does not apply at Gen 4 speed. It is performed at Gen 3 speed if supported by the UUT. Otherwise the test is performed at Gen 2 speed.*

A. Purpose:

- Verify that the PUT receiver can operate with maximum skew

B. Asserts:

- 4.4.4#1

C. Test Setups

- EX\_HOST\_DFP1 (Host)
- EX\_DEV\_UFP1 (Device)
- EX\_HUB\_UFP1 (Hub UFP)
- EX\_HUB\_DFP1 (Hub DFP)

D. Repetitions:

- Repeat at Gen 2 and Gen 3 speeds (if supported)
- Repeat test 5 times with Lane 0 skewed ahead of Lane 1
- Repeat test 5 times with Lane 1 skewed ahead of Lane 0

E. Background Check:

- Lane 0/Lane 1 Background Check

F. Procedure:

*Note: Throughout this test, the Exerciser inserts a static skew between Lane 0 and Lane 1 of up to 44ns on the Link with the UUT.*

*Note: When performing this test on an UFP, the exerciser performs both the test steps that are defined “Upstream of the UUT”. When this test is performed on a DFP, USB4 CV performs the tests steps that are defined “Upstream of the UUT”.*

Upstream of the UUT:

1. Reset UUT to start Lane Initialization
2. Read the *Logical Layer Errors* field to reset the bits to 0b
3. Set bit 4 in the *Logical Layer Errors Enable* field to 1b to enable De-Skew Buffer Error reporting.
4. Initiate Lane Bonding
5. Wait 5 seconds
6. Send the Target Adapter a Read Request to read the *Logical Layer Errors* field in Adapter Configuration Space
7. Verify that bit 4 in the *Logical Layer Errors* field is 0b (i.e. there are no De-Skew Buffer errors) (4.4.4#1)

## TD 4.052 Reserved Values in Transactions Test

### A. Purpose:

- Verify that the PUT ignores a Transaction with an undefined value in a field
- Verify that the PUT ignores a Transaction with a non-zero value in a reserved field

### B. Asserts:

- 1.7#2, 1.7#6

### C. Test Setups

- EX\_HOST\_DFP1 (Host)
- EX\_DEV\_UFP1 (Device)
- EX\_HUB\_UFP1 (Hub UFP)
- EX\_HUB\_DFP1 (Hub DFP)

### D. Background Check:

- Sideband Channel Background Check

### E. Procedure:

*Note: When performing this test on an UFP, the exerciser performs both the test steps that are defined “Upstream of the UUT” and the test steps that are defined “On the PUT”. When this test is performed on a DFP, USB4 CV performs the tests steps that are defined “Upstream of the UUT” and the Exerciser performs the test steps that are defined “On the PUT”.*

Upstream of the UUT:

#### Part 0 - Setup

1. Reset UUT
2. Enumerate UUT Router
3. Initiate Lane Bonding

On the PUT:

#### Part 1 – Undefined Values

4. Wait for Lane Bonding to complete
5. Send the PUT an LT Transaction with  $LSESymbol = 110b$  (undefined) on Lane 0
6. Verify that the Adapters in the PUT do not transition out of CL0 state (1.7#2)
7. Send the PUT an LT Transaction with  $LSESymbol = 001b$  (undefined) on Lane 0
8. Verify that the Adapters in the PUT do not transition out of CL0 state (1.7#2)

#### Part 2 – Reserved Values

9. Send the PUT an AT Transaction on Lane 0 with:
  - a.  $CmdNotResp = 1b$  (Command)
  - b.  $Bit\ 5 = 1b$  (Rsvd)
  - c.  $REG = 0$  (Vendor ID)
  - d.  $LEN = 4$
  - e.  $WnR = 0b$  (Read)
10. Verify that the PUT sends an AT Response (1.7#6)

11. Send the PUT an LT Transaction on Lane 0 with:

- a. LSESymbol = LT\_Fall
- b. Bit 4 = 1b (Rsvd)

12. Verify that the PUT Adapters go to the CLd State (1.7#6)

Note: The way to detect the PUT Adapters are in CLd is to make sure the Sideband channel was Disconnected.

#### TD 4.109 Invalid CELSE Test

*Note: This test only applies to a PUT that supports USB4 Ver. 2.*

A. Purpose:

- Verify that the PUT checks CELSE symbols
- Verify that the PUT drops a Transaction with an invalid CELSE

B. Asserts:

- 

C. Test Setups

- EX\_HOST\_DFP1 (Host)
- EX\_DEV\_UFP1 (Device)
- EX\_HUB\_UFP1 (Hub UFP)
- EX\_HUB\_DFP1 (Hub DFP)

D. Procedure:

*Note: When performing this test on an UFP, the exerciser performs both the test steps that are defined “Upstream of the UUT” and the test steps that are defined “On the PUT”. When this test is performed on a DFP, USB4 CV performs the tests steps that are defined “Upstream of the UUT” and the Exerciser performs the test steps that are defined “On the PUT”.*

Upstream of the UUT:

Part 0 - Setup

1. Reset UUT
2. Enumerate UUT Router
3. Initiate Lane Bonding
4. Wait for Lane Bonding to complete

On the PUT:

Part 1 - Recovery

5. Enable Gen 4 Recovery flow
6. Send an ELT\_Recovery Transaction to the PUT
  - a. Transaction has an invalid CELSE
7. Verify that the Link remains in CL0

#### TD 4.110 Gen 4 CL1/2 Errors Test (with or without Re-timers)

*Note: This test only applies to a PUT that supports Gen 4 speed.*

F. Purpose:

- Verify that the PUT enters CL1/2 state correctly
  - Verify that the PUT exits CL1/2 state correctly
- G. Asserts:
- 
- H. Test Setups
- AN\_HOST\_DFP1 (Host)
  - AN\_DEV\_UFP1 (Device)
  - AN\_HUB\_UFP1 (Hub UFP)
  - AN\_HUB\_DFP1 (Hub DFP)
- F. Repetitions:
- Repeat with:
    - Errors
      - i. Send wrong index in CL\_OFF Ordered Sets
- G. CLx State in CL\_OFF Ordered Sets 1/2/0(error)
- ii. Transmit LFPS on Transmitter 1
  - iii. No LFPS response (Part 3)
    - Re-timers on Link
  - Repeat with:
    - EXIT\_TIME =
    - EXIT\_TIME = 5 minutes
    - Symmetric
- H. Asymmetric 3 transmitter
- I. Asymmetric 3 receivers
- I. Procedure:

USB4 CV performs the following steps:

#### Part 0 - Setup

1. Reset UUT
2. Enumerate UUT Router
3. Read the CL1/2 Support bit in the PUT
4. Do not enable Time Sync Handshakes
5. Enable CLx states in the PUT:
  - a. CL2 Enable = 0/1b
  - b. CL1 Enable = 1/0b
  - c. CL0s Enable = 1b
6. Enable CLx states in the Link Partner:
  - a. CL2 Enable = 0/1b
  - b. CL1 Enable = 1/0b
  - c. CL0s Enable = 1b

#### Part 1 – PUT Sends CL\_OFF while in CL0

7. Verify that the PUT sends at least 24 CL\_OFF Ordered Sets with index field set to 0 and CLx state field set to 1/2t.
8. Verify that the PUT sends 102 CL\_OFF Ordered Sets or valid Data Sets
9. If there are Re-timers on the Link repeat the following steps for each Re-timer i=1..number of Re-timers:
  - a. Verify that the PUT sends at least 24 CL\_OFF Ordered Sets with index field set to i and CLx state field set to 1/2t.
  - b. Verify that the PUT sends 102 CL\_OFF Ordered Sets or valid Data Sets
10. Verify that the PUT is in CL0s (Tx) state

11. Verify that transmitter is in electrical idle
12. Continue to Part 2

#### Part 2 – Exerciser Sends CL\_OFF

13. Exerciser sends 24 CL\_OFF Ordered Sets with Index field set to 0t or error (see repetitions) and CLx state set to 1/2t or error (see repetitions), followed by 102 valid Data Sets. No Redundancy Sets are sent
14. If there are Re-timers on the Link, the Exerciser sends the following for each Re-timer  $i=1..number\ of\ Re-timers$ :
  - a. Exerciser sends at least 24 CL\_OFF Ordered Sets with index field set to  $i$  or error (see repetitions) and CLx state field set to 1/2t or error (see repetitions).
  - b. Exerciser sends 102 CL\_OFF Ordered Sets or valid Data Sets
15. Verify that the PUT enters CL2 state
16. Continue to Part 3 or Part 4 (see repetitions)

#### Part 3 – PUT initiating CL2 Exit

17. Wait for PUT to transmit LFPS on Transmitter 0.
18. Exerciser waits for 1s before transmitting LFPS
19. Verify that PUT doesn't initiate Disconnect before tTrainingAbort2

#### Part 4 – Exerciser initiating CL2 Exit

20. Wait EXIT\_TIME time after detecting that the PUT transitioned to CL2 state (see repetitions)
21. Transmit LFPS on Transmitter 0 or Transmitter 1 (see repetitions).
22. If LFPS was transmitter on Transmitter 0, verify that the PUT does the following:
  - a. Sends an LFPS burst on Lane 0 for at least 16 LFPS cycles
  - b. Stop sending LFPS tStopLFPS2 after sending at least 16 LFPS cycles and LFPS ended on its receiver
  - c. Sends the first LFPS within tWarmUpCL2 after receiving the first LFPS cycle
  - d. Returns to Electrical Idle for tPreData
  - e. Starts transmitting Gen 4 TS1 on all the enabled Lanes
  - f. Enables the receiver to start bit and symbol synchronization not earlier than tCLxIdleRx after the last LFPS cycle received
  - g. Completes Symbol lock within tRxLock time
23. Verify that the PUT transitions to CL0 state

### TD 4.115 Gen 4 CL0s Errors Test (with or without Re-timers)

- A. Purpose:
  - Verify that the PUT Adapters enter CL0s state correctly
  - Verify that the PUT Adapters exit CL0s state correctly
- B. Asserts:
  -
- C. Test Setups
  - EX\_HOST\_DFP1 (Host)
  - EX\_DEV\_UFP1 (Device)
  - EX\_HUB\_UFP1 (Hub UFP)
  - EX\_HUB\_DFP1 (Hub DFP)
- D. Repetitions:
  - With/without Re-timers
  - Symmetric
  - Asymmetric 3 transmitter

- Asymmetric 3 receivers
  - Errors
    - a. Send wrong index in CL\_OFF Ordered Sets
    - b. CLx State in CL\_OFF Ordered Sets 1/2/0(error)
    - c. Transmit LFPS on Transmitter 1
    - d. Halting CL0s Exit flow in TS1/TS2/TS3 states
  - Repeat with:
    - EXIT\_TIME = 5us
    - EXIT\_TIME = 30 seconds
- E. Gen 4 Background Check
- F. Procedure:

USB4 CV performs the following steps:

#### Part 0 - Setup

1. Reset UUT
2. Enumerate UUT Router
3. Enable CLx states in the PUT and the Exerciser:
  - a. *CL2 Enable* = 1b
  - b. *CL1 Enable* = 1b
  - c. *CL0s Enable* = 1b
4. Configure/enable unidirectional timestamps (HiFi mode) for objection to CL2/CL1 in the PUT

#### Part 1 – Initiate CL0s Entry

5. Exerciser sends 24 CL\_OFF Ordered Sets with Index field set to 0t or error (see repetitions) and CLx state set to 1/2t or error (see repetitions), followed by 102 valid Data Sets. No Redundancy Sets are sent
6. If there are Re-timers on the Link, the Exerciser sends the following for each Re-timer  $i=1..number\ of\ Re-timers$ :
  - a. Exerciser sends at least 24 CL\_OFF Ordered Sets with index field set to i or error (see repetitions) and CLx state field set to 1/2t or error (see repetitions).
  - b. Exerciser sends 102 CL\_OFF Ordered Sets or valid Data Sets
7. Verify that the PUT enters CL0s (RX) state

#### Part 2 – Initiate CL0s Exit

18. Exerciser transmitting LFPS on Transmitter 1
19. Verify that PUT doesn't respond
20. Exerciser transmits LFPS on Transmitter 0
21. Verify that the PUT sends CL0s\_EXIT Ordered Set with CL0s\_Phase field set to 0t within tTrainingTransition time
22. Exerciser goes to Electrical Idle for tPreData and then transmits TS1 with indication 2h
23. Verify that the PUT sends CL0s\_EXIT Ordered Set with CL0s\_Phase field set to 01t within tTrainingTransition time
24. Exerciser halts (see repetitions) or transmits TS2 with indication 4h
25. Verify that the PUT sends CL0s\_EXIT Ordered Set with CL0s\_Phase field set to 02t within tTrainingTransition time
26. Exerciser halts (see repetitions) or execute the Clock Switch flow and after it transmits TS3 with indication 5h

27. Verify that the PUT sends CL0s\_EXIT Ordered Set with CL0s\_Phase field set to 03t within tTrainingTransition time
28. Exerciser halts (see repetitions) or transmits TS4 with Counter field increasing from 0 to Fh, then it activates pre-coding, scrambling and RS-FEC coding. The first RS-FEC block it transmits is the De-skew Block.
29. Verify the PUT is in CL0 and have a working Link.
30. If the exerciser halts in one of the steps, verify that the PUT doesn't initiate Disconnect before tTrainingAbort2 time passed.

#### TD 4.144 Gen 4 RS-FEC Correctable Error Test

##### G. Purpose:

- Verify that the PUT can correct up to 12 1-byte-symbol errors in an RS-FEC block

##### H. Asserts:

- 

##### I. Test Setups

- EX\_HOST\_DFP1 (Host)
- EX\_DEV\_UFP1 (Device)
- EX\_HUB\_UFP1 (Hub UFP)
- EX\_HUB\_DFP1 (Hub DFP)

##### J. Repetitions:

- Symmetric
- Asymmetric 3 transmitter
- Asymmetric 3 receivers

##### K. Background Check:

- Gen 4 Background Check

##### L. Procedure:

USB4 CV performs the following steps:

11. Reset UUT
12. Tell the Exerciser to generate correctable errors

*Note: The Exerciser injects randomly spaced errors so that up to 12 errors fall within an RS-FEC block*

13. Enumerate the UUT Router
14. Verify that the PUT sends a Read Response for each Read Request it receives (4.3.6#13)
15. Verify that the Lane Adapters on either side of the Link are in CL0 state
16. Read bit 5 (RS-FEC Decoder Error) in the *Logical Layer Errors* field
17. Verify that bit 5 (RS-FEC Decoder Error) in the *Logical Layer Errors* field is 0b (4.3.6#13)
18. Verify that the Link does not go down at any time while the Exerciser is generating correctable errors (4.3.6#13)



## TBT3-Compatibility Tests – No Exerciser

The tests in this section are performed in TBT3-Compatible mode where all connected Ports negotiate and enter TBT3-Compatible operation as described in the USB Type-C Specification and the USB PD Specification.

Unless specified otherwise, the tests in this section are performed on all Ports of a UUT. The tests are performed at Gen 3 speed if supported by the UUT. Otherwise tests are performed at Gen 2 speed. Lanes are bonded and RS-FEC is enabled.

Unless otherwise noted, a test will timeout if it takes more than 500ms to go from one step to the next step. It is a test failure if a test times out.

### Background Checks

#### Sideband Channel Background Check

This test is performed by the Analyzer in conjunction with all of the Sideband Channel Tests if the Sideband Channel between the UUT and the TBT3 Compliance Device is TBT3.

1. Parse each LT Transaction and verify that it consists of the following symbols in the following order: (4.1.1.2.1#1)
  - a. A DLE symbol (FEh)
  - b. A LSE symbol
  - c. A CLSE symbol
2. Parse the LSE Symbol in each LT Transaction and verify that:
  - a. Bits [7:6] (*StartLT*) are set to 10b (4.1.1.2.1#4)
  - b. Bit 5 (*LSELane*) is 0 for an LT\_LRoff Transaction (4.1.1.2.1#3)
  - c. Bit 4 is reserved (0b) (1.7#5)
  - d. Bits [3:0] (*LSESymbol*) do not contain reserved values (1.7#1)

*Note: Defined LSESymbol values are 0000b (LT\_Fall), 0001b (LT\_Gen\_2), 0010b (LT\_Resume), 0011b (LT\_LRoff), 0101b (LT\_Gen\_3), 0110b (LT\_Resume2)*
3. Parse each AT Transaction and verify that it consists of the following symbols in the following order: (4.1.1.2.2#1)
  - a. A DLE symbol (FEh)
  - b. A STX symbol
  - c. No more than 66 Data Symbols (4.1.1.2.2#2)
  - d. 2 CRC Symbols (Low and High) with correct CRC (4.1.1.2.4#5, 4.1.1.2.4#6, 4.1.1.2.4#7, 4.1.1.2.4#8, 4.1.1.2.4#9)
  - e. A DLE symbol (FEh)
  - f. An ETX symbol (40h)
4. For each AT Command:
  - a. Parse the STX Symbol and verify that: (13.2.1.2.2#1)
    - i. Bits [7:6] (*StartAT*) are 00b
    - ii. Bit 5 is reserved (0b) (1.7#5)
    - iii. Bit 4 (*Responder*) is 0b (13.2.1.2.2#3)
  - b. Parse the Data Symbols and verify that: (4.1.1.3.1#1)
    - i. The REG symbol does not contain the values 2, 5 to 7, 11, 14, or 128 to 255
    - ii. The LEN symbol does not contain a value greater than 64 (4.1.1.3.1#2)
    - iii. If WnR=0, there is no COMMAND\_DATA
    - iv. If WnR=1b, the COMMAND\_DATA is the same length as in the LEN field

5. For each AT Response:
  - a. Parse the STX Symbol and verify that: (13.2.1.2.2#1)
    - i. Bits [7:6] (*StartAT*) are 00b
    - ii. Bit 5 is reserved (0b) (1.7#5)
    - iii. Bit 2 (*Recipient*) is 1b (13.2.1.2.2#5)
  - b. Parse the Data Symbols and verify that they consist of the following symbols in the following order: (4.1.1.3.1#2)
    - i. A REG symbol does not contain the values 2, 5 to 7, 11, 14, or 128 to 255
    - ii. A LEN symbol does not contain a value greater than 64 (4.1.1.3.1#2)
    - iii. If WnR=0b, RESPONSE\_DATA is the same length as in the LEN field (unless test specifies otherwise)
    - iv. If WnR=1n, RESPONSE\_DATA is 00h (unless test specified otherwise)
  - c. Verify that the value in the LEN field is not greater than 64 (4.1.1.3.1#2)
6. When the PUT receives an AT Command with the Recipient bit set to 1b, verify that the PUT responds with an AT Response (unless the test specifies otherwise). (4.1.1.2.2#9)
7. Parse each Broadcast RT Transaction and verify that it consists of the following symbols in the following order: (4.1.1.2.3.1#1)
  - a. A DLE symbol (FEh)
  - b. A STX symbol
  - c. Two Link Parameters symbols
  - d. 2 CRC Symbols (Low and High) with correct CRC (4.1.1.2.4#5, 4.1.1.2.4#6, 4.1.1.2.4#7, 4.1.1.2.4#8, 4.1.1.2.4#9)
  - e. A DLE symbol (FEh)
  - f. An ETX symbol (40h)
8. Parse the STX Symbol for a Broadcast RT Transaction and verify that:
  - a. *Index* = 0 (4.1.1.2.3.1#4)
  - b. *CmdNotResp*=1b (4.1.1.2.3.1#5)
9. Parse Byte 2 of a Broadcast RT Transaction and verify that:
  - a. Bits [7:5] are 0 (reserved) (1.7#5)
  - b. Bit 4 (*TBTCompatibleSpeed*) is 1b (13.2.1.2.3#1)
  - c. Bit 1 (reserved) is 0b (1.7#5)
  - d. Bit 0 (*USB4*) is 0b (13.2.1.2.3#1)
10. Parse each Addressed RT Transaction and verify that it consists of the following symbols in the following order: (4.1.1.2.3.2#1)
  - a. A DLE symbol (FEh)
  - b. A STX symbol
  - c. No more than 66 Data Symbols (4.1.1.2.3.2#2)
  - d. 2 CRC Symbols (Low and High) with correct CRC (4.1.1.2.4#5, 4.1.1.2.4#6, 4.1.1.2.4#7, 4.1.1.2.4#8, 4.1.1.2.4#9)
  - e. A DLE symbol (FEh)
  - f. An ETX symbol (40h)
11. Parse the Data Symbols of each RT Command and verify that it consists of the following symbols in the following order: (4.1.1.3.1#1)
  - a. The REG symbol does not contain the values 2, 5 to 7, 11, 14, or 128 to 255
  - b. The LEN symbol does not contain a value greater than 64
  - c. If WnR=0, there is no COMMAND\_DATA
  - d. If WnR=1b, the COMMAND\_DATA is the same length as in the LEN field
12. Parse the Data Symbols of each RT Response and verify that it consists of the following symbols in the following order: (4.1.1.3.1#2)

- a. The REG symbol does not contain the values 2, 5 to 7, 11, 14, or 128 to 255
  - b. The LEN symbol does not contain a value greater than 64 (4.1.1.3.1#2)
  - c. If WnR=0b, RESPONSE\_DATA is the same length as in the LEN field (unless test specifies otherwise)
  - d. If WnR=1n, RESPONSE\_DATA is 00h (unless test specified otherwise)
13. Verify that the PUT sends an AT Response within tCmdResponse (50ms) of receiving an AT Command. (4.1.1.2.5.1#1)
  14. Verify that the PUT sends an Addressed RT Response within tCmdResponse (50ms) of receiving an Addressed RT Command. (4.1.1.2.5.2#1)

### Lane 0/Lane1 Background Check

This test is performed by the or Exerciser in conjunction with all of the Lane 0/Lane 1 Tests.

1. Parse each TS1 and TS2 Ordered Set and verify that bits 31:29 (Rsvd) are 0. (4.2.1.3.5#6)
2. When an Adapter transitions to the CL0 state and Lanes are not bonded, verify that the first bytes transmitted after the last TS2 Ordered Set are either a Transport Layer Packet header or an Ordered Set that is not SLOS, TS1, or TS2. (4.4.1#1)
3. When an Adapter transitions to the CL0 state and Lanes are bonded, verify that the first bytes transmitted after the last TS2 Ordered Set are a de-skew Ordered Set followed by either a Transport Layer Packet header, an Idle Packet or any Ordered Set other than SLOS, TS1 or TS2. (4.4.1#2)
4. When operating with a Dual-lane Link, verify that, if one Lane transitions to Training State, other Lane also transitions to training state (4.2.2.2#8)

## Test Descriptions

### TD 13.1.001 Bounce Mechanism Test

*Note: This test is only performed with an Active Cable that contains re-timers.*

- A. Purpose:
  - Verify that the Bounce Mechanism is performed correctly
- B. Asserts:
  - 13.2.1.2.2.1#1-4
- C. Test Setups
  - AN\_HOST\_DFP1—TBT3\_01 (Host)
  - AN\_DEV\_UFP1—TBT3\_01 (Device)
  - AN\_HUB\_UFP1—TBT3\_01 (Hub UFP)
  - AN\_HUB\_DFP1—TBT3\_03 (Hub DFP)
- D. Background Check:
  - Sideband Channel Background Check
- E. Procedure:

USB4 performs the following steps:

#### Part 0 – Setup

1. Reset UUT
2. Perform Lane Initialization
3. Initiate Lane Bonding

#### Part 1 – Link Partner

4. Tell the UUT to send a Write Command to the Re-timer that is adjacent to the Link Partner
5. Verify that a Write Response is received
6. Tell the UUT to send a Read Command to the Re-timer that is adjacent to the Link Partner
7. Verify that a Read Response is received
8. Verify that the data in the Read Response is the same as what was written

#### Part 2 – Adjacent Re-Timer

9. Tell the Link Partner to send a Write Command to the Re-timer that is adjacent to the UUT
10. Verify that a Write Response is received
11. Tell the Link Partner to send a Read Command to the Re-timer that is adjacent to the UUT
12. Verify that a Read Response is received
13. Verify that the data in the Read Response is the same as what was written

#### TD 13.1.002 SB Register Space Test

- A. Purpose:
  - Verify that SB Register space is formatted correctly
- B. Asserts:
  - 13.2.1.3#1
- C. Test Setups
  - AN\_HOST\_DFP1—TBT3\_01 (Host)
  - AN\_DEV\_UFP1—TBT3\_01 (Device)
  - AN\_HUB\_UFP1—TBT3\_01 (Hub UFP)
  - AN\_HUB\_DFP1—TBT3\_03 (Hub DFP)
- D. Background Check:
  - Sideband Channel Background Check
- E. Procedure:

USB4 performs the following steps:

##### Part 0 – Setup

1. Reset UUT
2. Perform Lane Initialization
3. Initiate Lane Bonding
4. Read SB Registers, 3, 4, and 10
5. In SB Register 3, verify the following values:
  - a. Byte 0 = 41h
  - b. Byte 1 = 50h
  - c. Byte 2 = 50h
  - d. Byte 3 = 20h
6. In SB Register 4, verify the following values:
  - a. Byte 0 = 45h
  - b. Byte 1 = 4Dh
  - c. Byte 2 = 20h
  - d. Byte 3 = 20h
7. In SB Register 10, verify that Byte 0 is 00h

### TD 13.1.003 Lane Initialization Test

- A. Purpose:
  - Verify that Lane Initialization is performed correctly in TBT3-Compatibility mode
- B. Asserts:
  - 13.2.1.4.4#1-8, 13.2.1.4.4.1#1-14, 13.2.1.4.4.2#1-13
- C. Repetitions:
  - Repeat with a TBT3 device that uses a:
    - TBT3 Sideband Channel Repeat at Gen 2 and Gen 3 speeds
  - Repeat with RS-FEC enabled and disabled
  - Repeat with the following cable types:
    - Passive Cable
    - Uni-Directional Active Cable that contains re-timers
    - Bi-Directional Active Cable that contains re-timers
- D. Test Setups
  - AN\_HOST\_DFP1—TBT3\_01 (Host)
  - AN\_DEV\_UFP1—TBT3\_01 (Device)
  - AN\_HUB\_UFP1—TBT3\_01 (Hub UFP)
  - AN\_HUB\_DFP1—TBT3\_03 (Hub DFP)
- E. Background Check:
  - Sideband Channel Background Check
- F. Procedure:

USB4 performs the following steps:

#### Part 0 – Setup

1. Reset PUT
2. Start Lane Initialization
3. In phase 4, verify the following:
  - a. If the is operating at Gen 2 speed, verify that:
    - i. UUT sends an LT\_Gen\_2 Transaction for each enabled Lane every tLaneParams (13.2.1.4.3#2)
    - ii. UUT continues sending LT\_Gen\_2 Transactions until all of the following are true: At least tLTPHase4 time has passed from completion of Phase 2; UUT sent LT\_Gen\_2 Transactions at least twice; UUT received an LT\_Gen\_2 Transaction (13.2.1.4.3#3)
  - b. If the UUT is operating at Gen 3 speed, verify that:
    - i. UUT sends an LT\_Gen\_3 Transaction for each enabled Lane every tLaneParams (13.2.1.4.3#4)
    - ii. UUT continues sending LT\_Gen\_3 Transactions until all of the following are true: At least tLTPHase4 time has passed from completion of Phase 2; UUT sent LT\_Gen\_3 Transactions at least twice; UUT received an LT\_Gen\_3 Transaction (13.2.1.4.3#5)
4. If the UUT is connected to an Active Cable with Re-timers, perform Asymmetric TxFFE Parameter Negotiation
5. Else perform Symmetric TxFFE Parameter Negotiation
6. In phase 5, verify the following:
  - a. If Asymmetric TxFFE Parameter Negotiation is performed:
    - i. UUT Transmitter sends an LT\_Resume2 Transaction for Lane 1 (LSELane field = 1b) (13.2.1.4.4#3)

- ii. UUT Transmitter sends an LT\_Resume2 Transaction for Lane 0 (LSELane field = 0b) (13.2.1.4.4#3)
- b. UUT sets the Clock Switch Done bit to 1b for Lane 1 (13.2.1.4.4#6)
- c. UUT sets the Clock Switch Done bit to 1b for Lane 0 (13.2.1.4.4#6)

#### TD 13.1.004     Single Lane Link Test (Hub DFP Only)

*Note: This test is only performed on the DFP of a Hub.*

*Note: This test is only performed if the UFP of the Hub supports TBT3-Compatibility.*

- A. Purpose:
  - Verify that the Single Lane Link configuration is supported
- B. Asserts:
  - 13.2.3.1#2
- C. Test Setups
  - AN\_HUB\_DFP1—TBT3\_03 (Hub)
- D. Background Check:
  - Lane 0/Lane1 Background Check
- E. Procedure:

USB4 performs the following steps:

##### Part 0 – Setup

1. Reset UUT
2. Perform Lane Initialization
3. Do not initiate Lane Bonding
4. Set up a loopback Path over Lane 0
5. Perform a loopback transfer
6. Verify that the loopback transfers complete without error (13.2.3.1#2)



TD 13.1.005      Deprecated

TD 13.1.006      Deprecated

TD 13.1.007      Deprecated